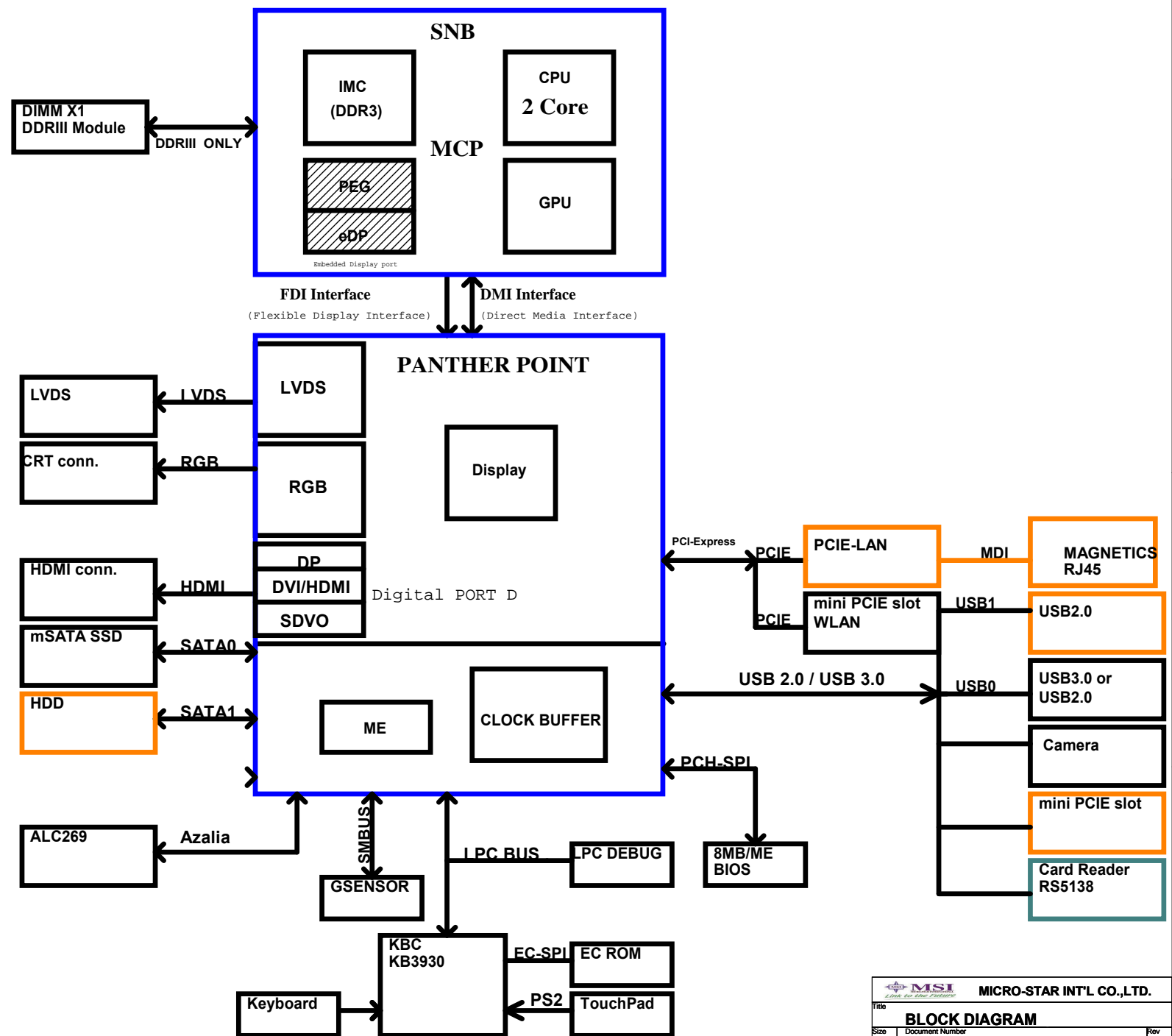



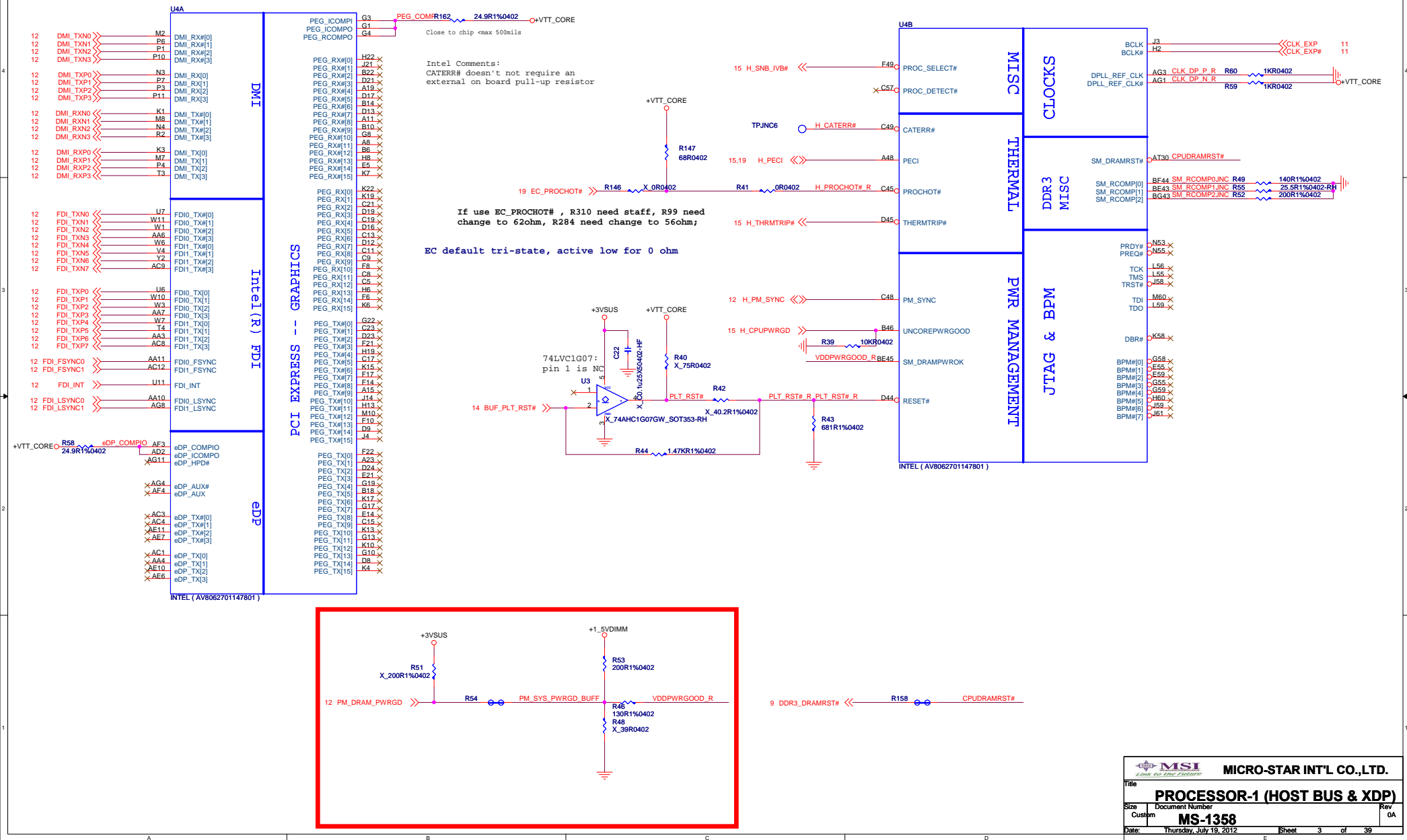
1358 VER :0A



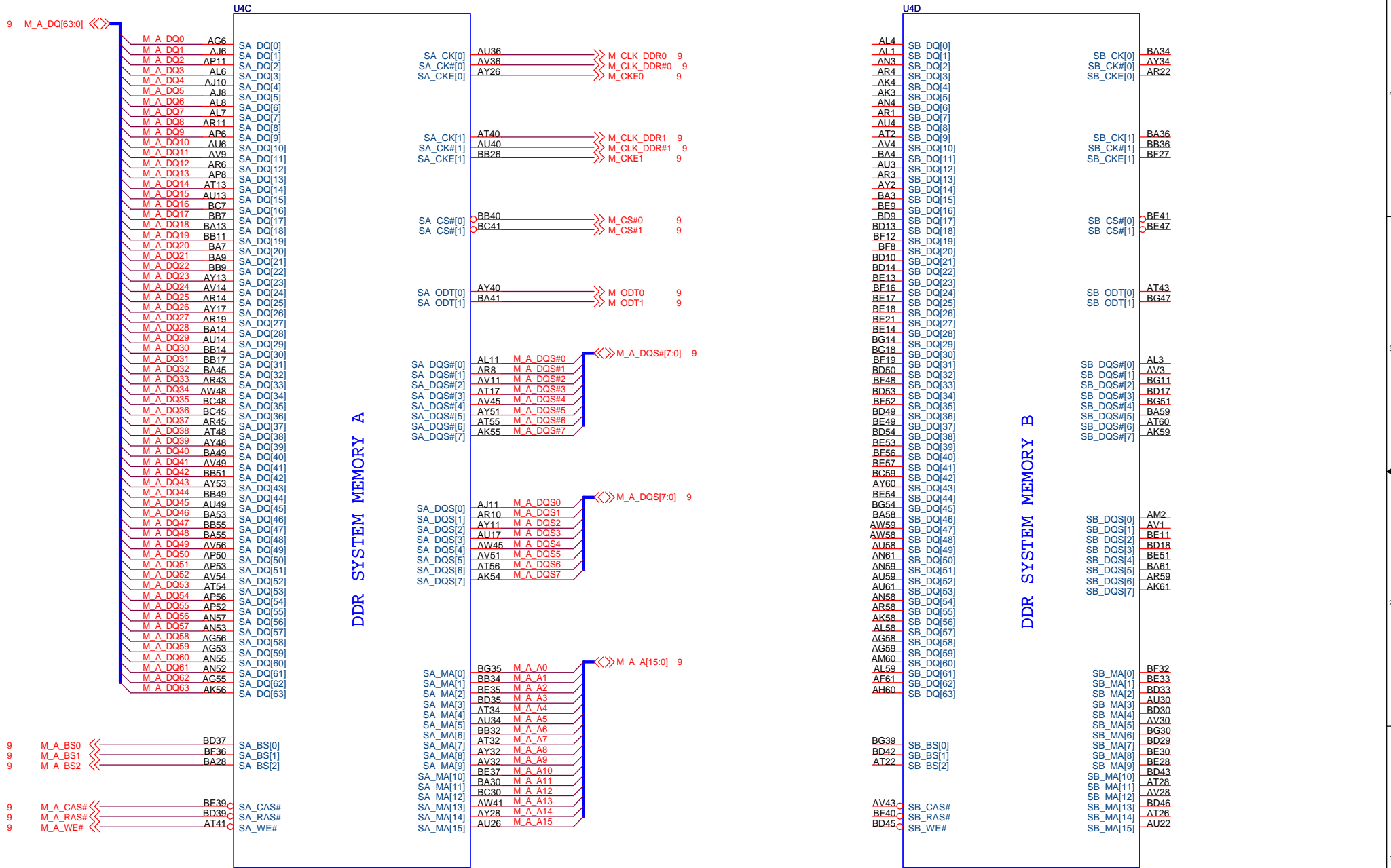
	A	B	C	D	E
1					
2					
3					
4					
	A	B	C	D	E


 MICRO-STAR INT'L CO.,LTD.	
PLATFORM	
Size Custom	Document Number MS-1358
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IVY BRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)



IVY BRIDGE 2C BGA PROCESSOR (DDR3)

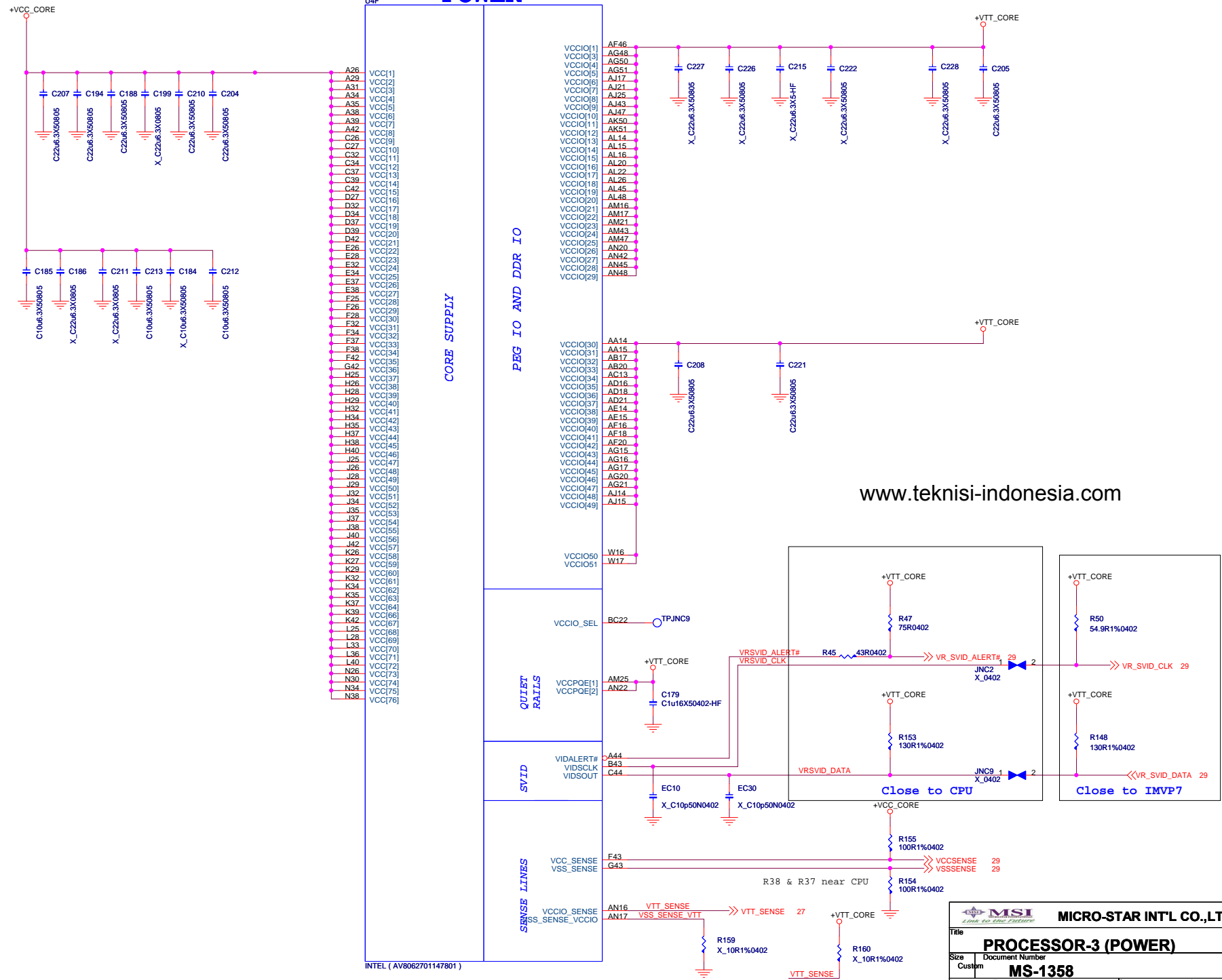


 MICRO-STAR INT'L CO.,LTD.	
PROCESSOR-2 (DDR3)	
Title Size Custom	Document Number MS-135X
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IVY BRIDGE 2C BGA PROCESSOR (POWER)

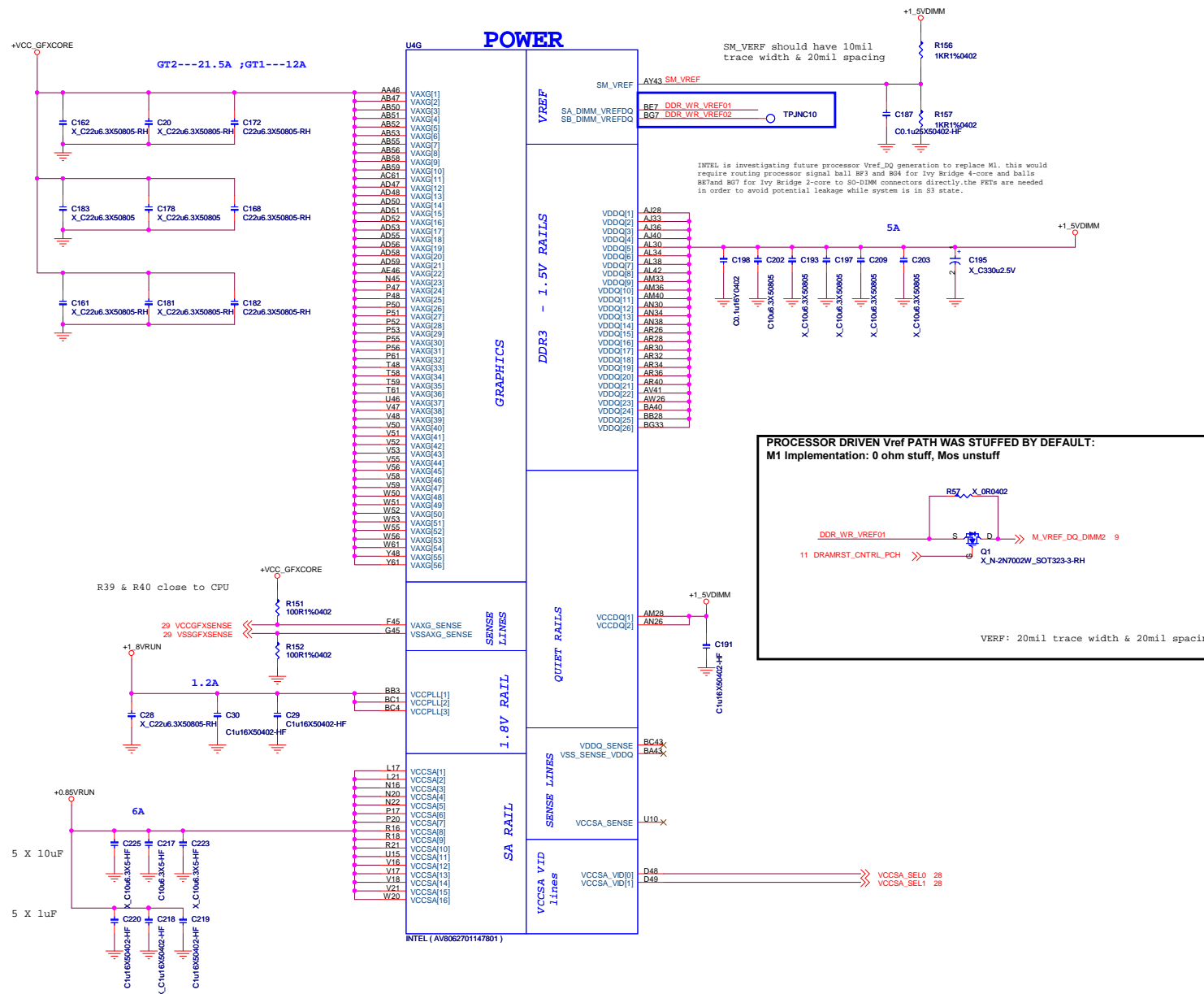
For SV CPU

POWER



INTEL (AV8062701147801)

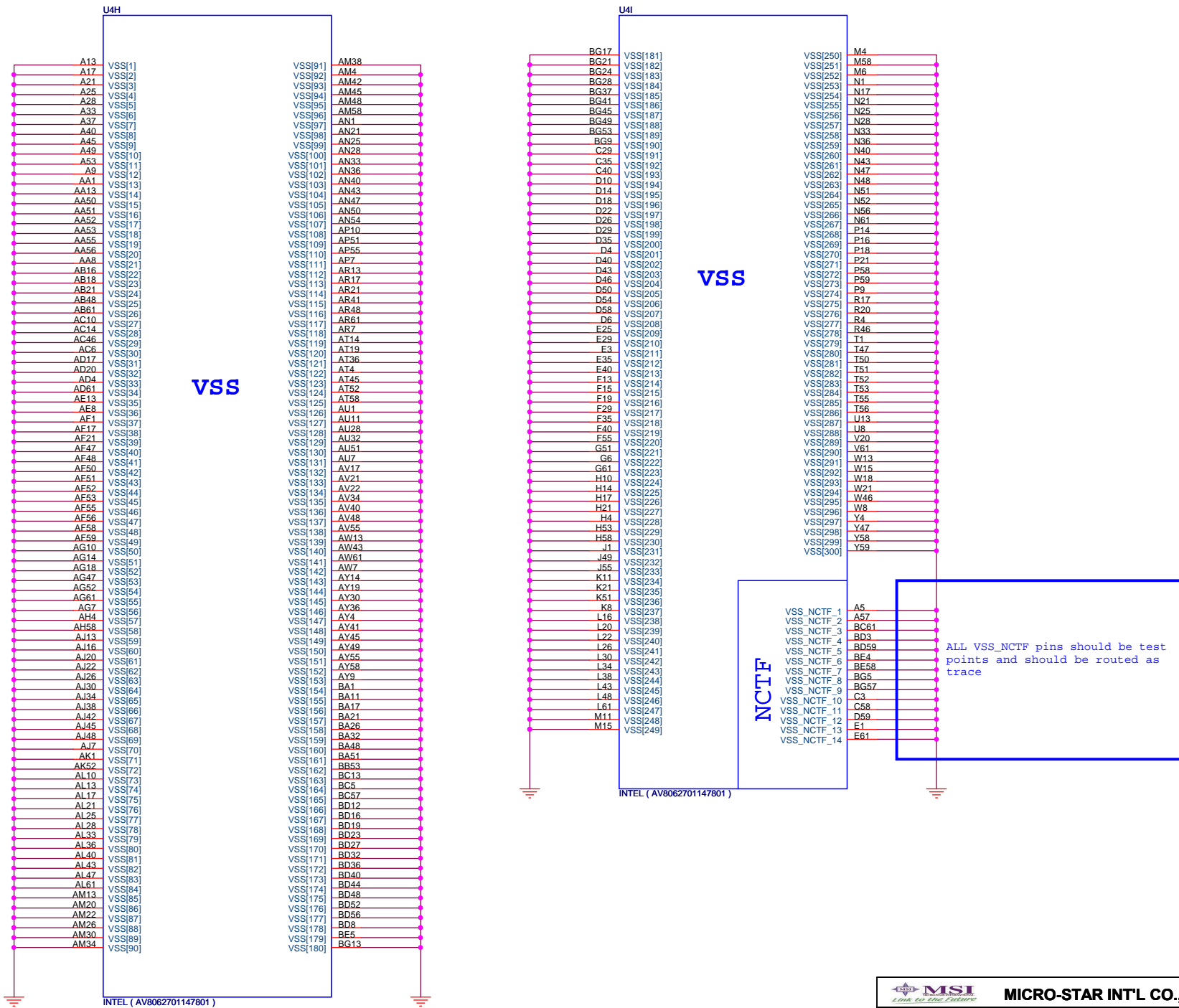
IVY BRIDGE 2C BGA PROCESSOR (GRAPHICS POWER)



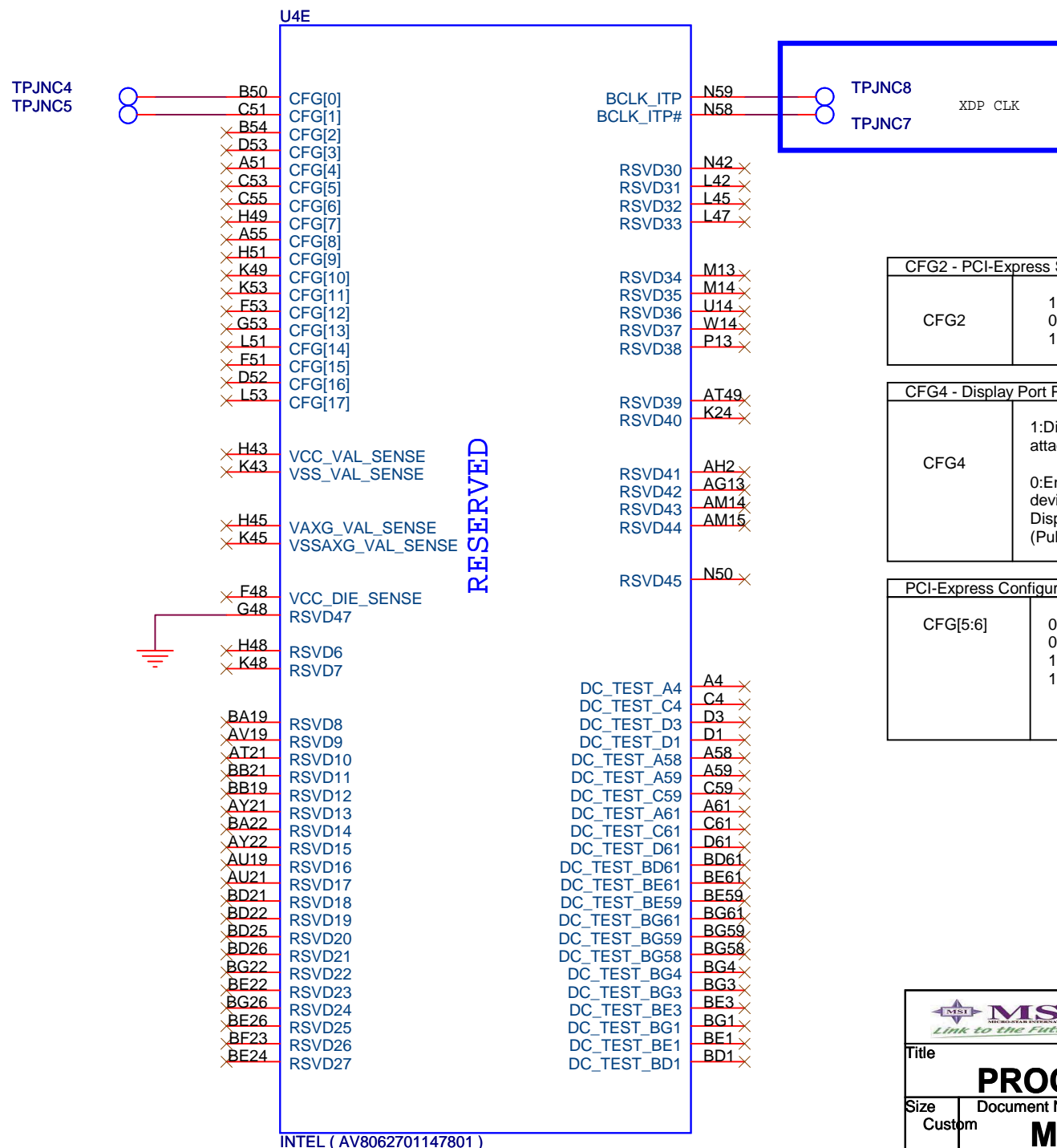
VCCSA_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	Required for 2011 processor	Required for 2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

IVY BRIDGE 2C BGA PROCESSOR (GND)




IVY BRIDGE 2C BGA PROCESSOR (RESERVED)



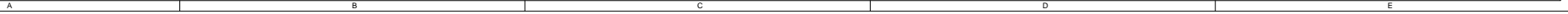
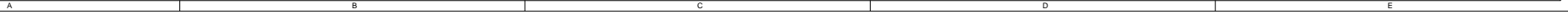
CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	<p>1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG)</p> <p>0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K \pm 5% resistor)</p>

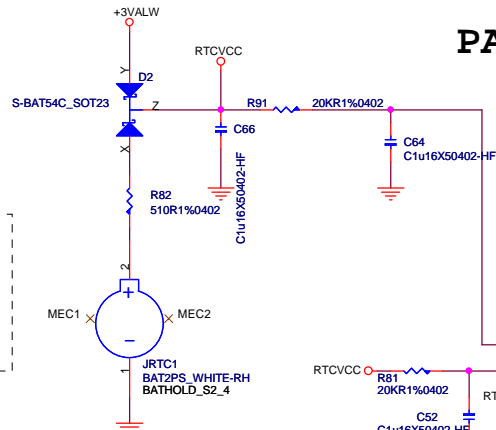
PCI-Express Configuration Select	
CFG[5:6]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express (Default)

		MICRO-STAR INT'L CO.,LTD.			
Title					
PROCESSOR-6 (RESERVE)					
Size Custom	Document Number MS-1358				Rev 0A
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A	B	C	D	E
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PANTHER POINT (HDA,JTAG,SATA)



N91-01F0270-L06

RTC Battery
D06-0101510-K26

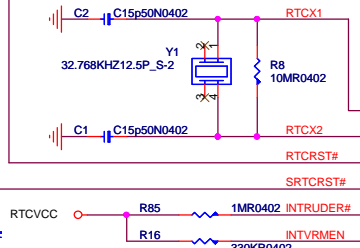
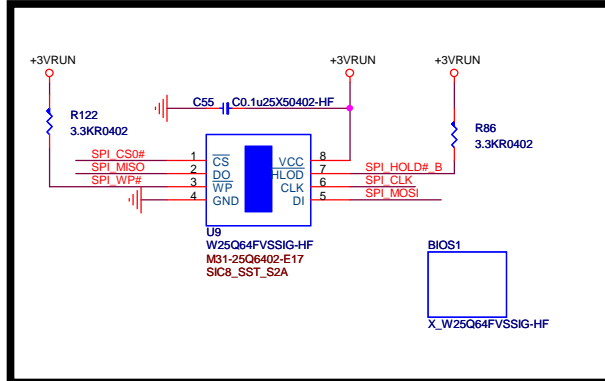
This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when sampled high, 1.8 V from VccVRM when sampled low.

HDA_SYNC	Low = On Die PLL VR is supplied by 1.8V High = On Die PLL VR is supplied by 1.5V
----------	---

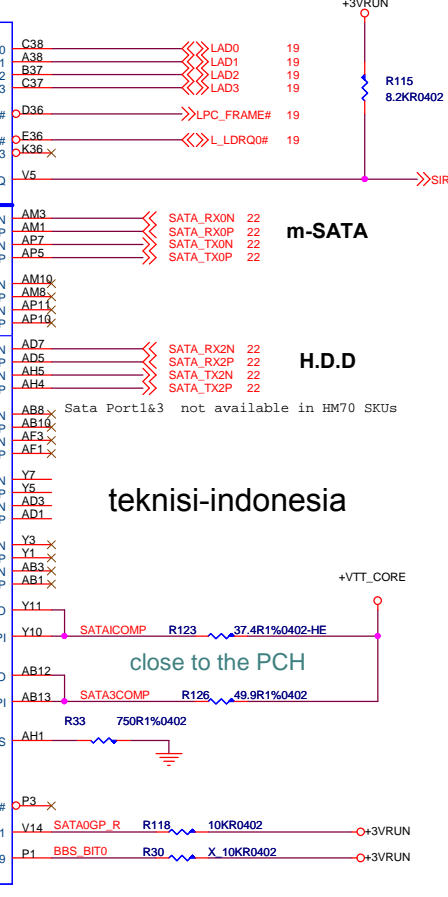
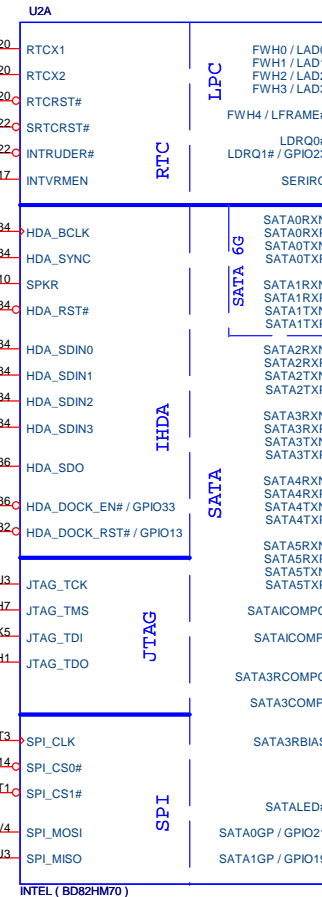
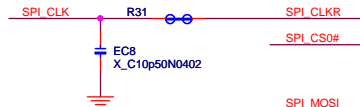
This signal has a weak internal pull-down.
The strap is sampled on the rising edge of RSMRST# signal.

Note: HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH. The strap is sampled on the rising edge of RSMRST# signal. Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input. Therefore, platform may need to isolate this signal from the codec during the strap phase. Refer to the example circuits provided in the latest Chief River platform design guide.

EEPROM

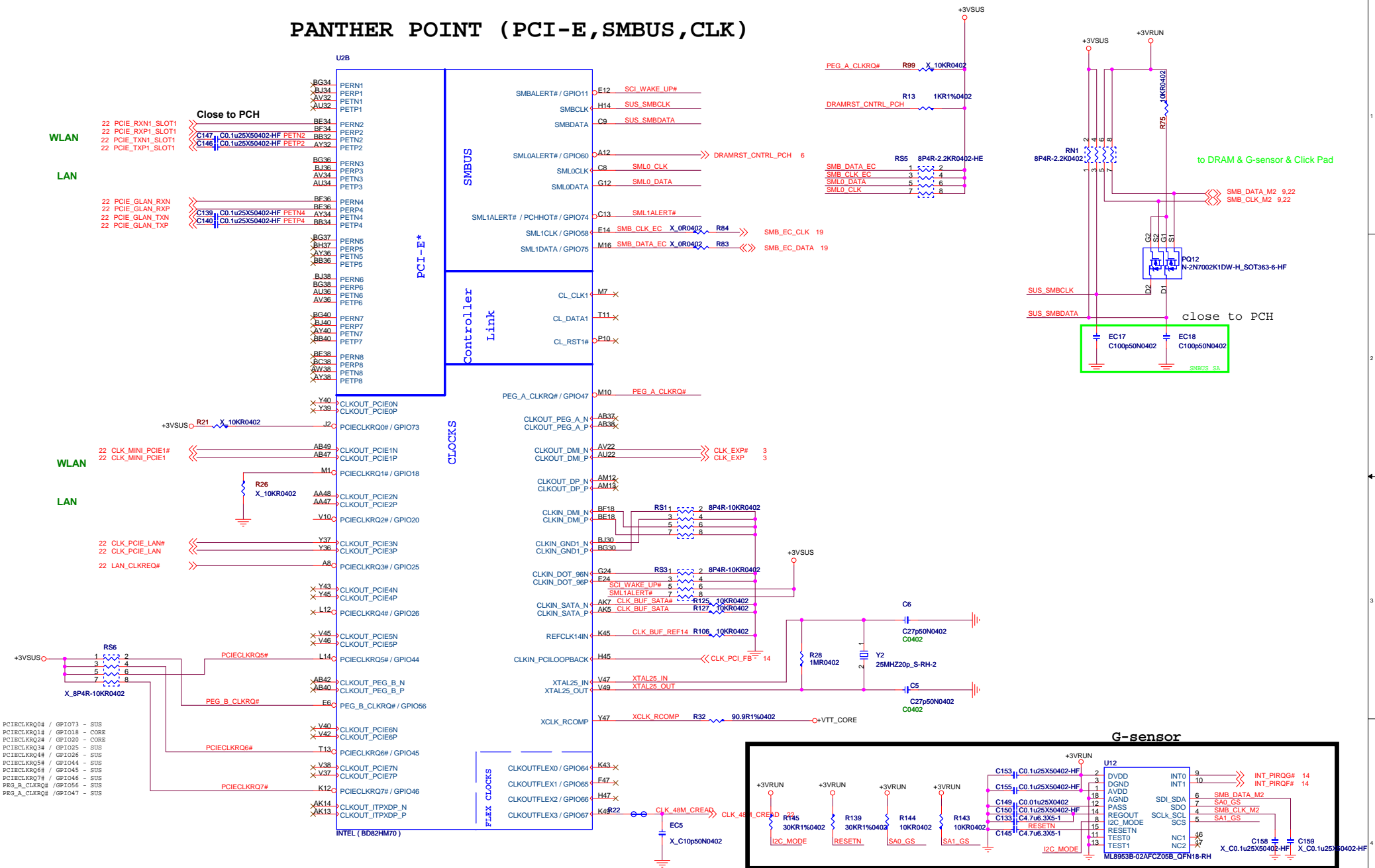


Flash Descriptor Security Protect	
HDA_SDO	High = overridden Low = Disable (Default)



SPK	The Signal has a weak internal pull-down Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)
-----	---

PANTHER POINT (PCI-E, SMBUS, CLK)

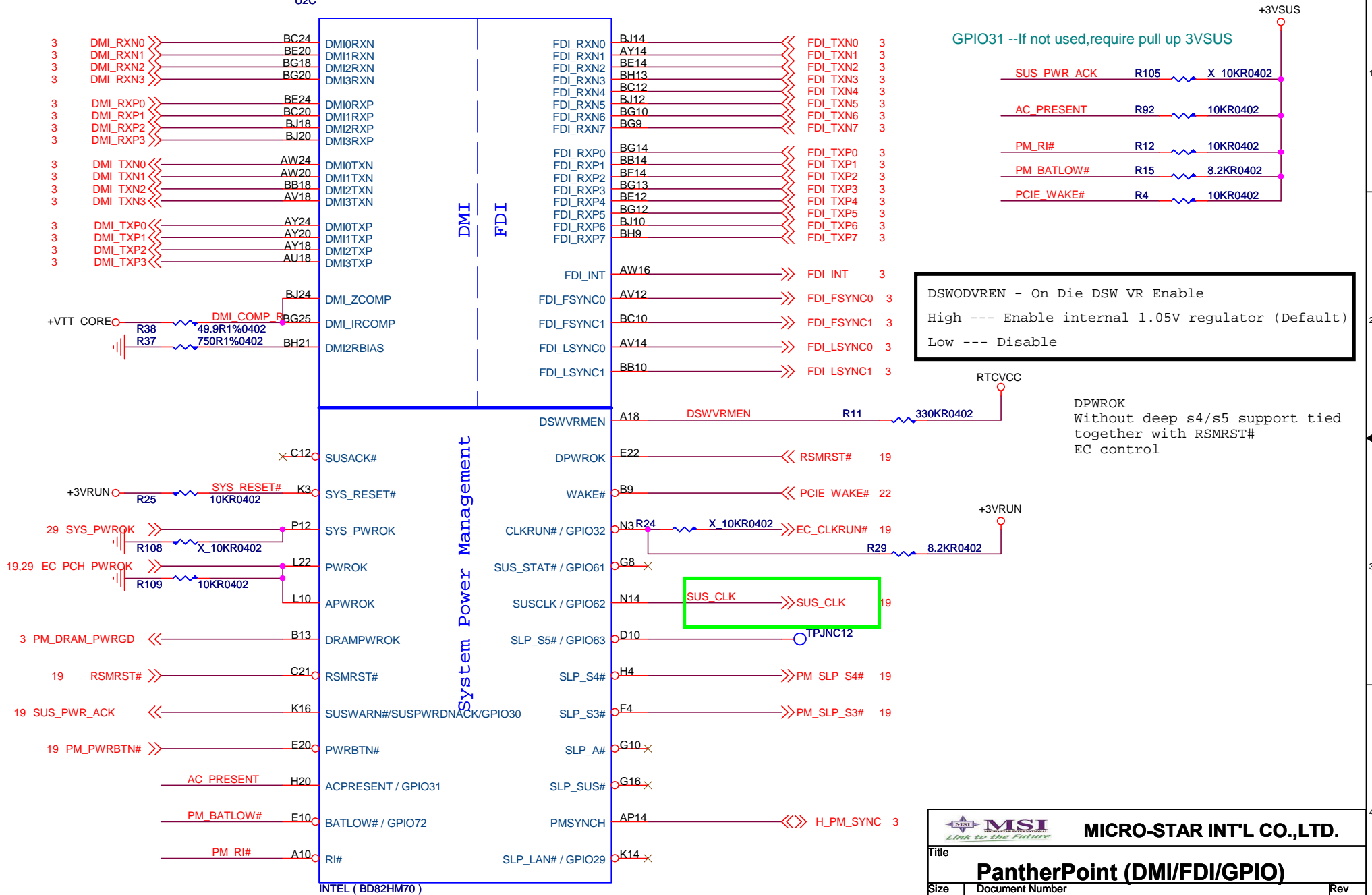



PCIe devices or add-in cards that do not support CLKREQ# functionality should not route this signal to PCH. Intel recommends terminating PCIECLKREQ# pin on PCH with 10 k \pm 10% external pull-up resistor instead of No Pull-Up. PCIECLKREQ#[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

Intel Comments:
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.

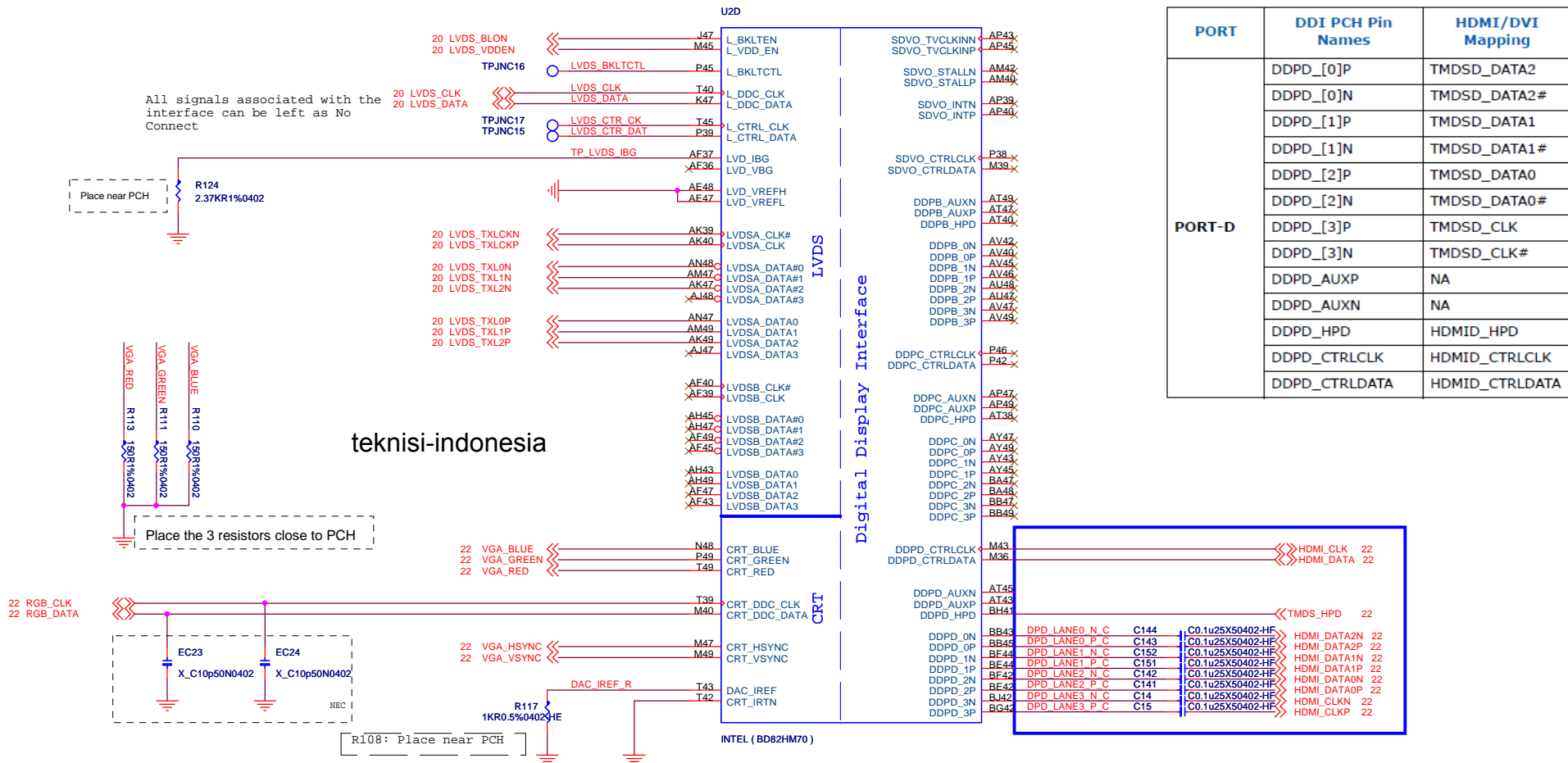
PANTHER POINT (DMI, FDI, GPIO)

U2C



 MICRO-STAR INT'L CO.,LTD.	
Title PantherPoint (DMI/FDI/GPIO)	
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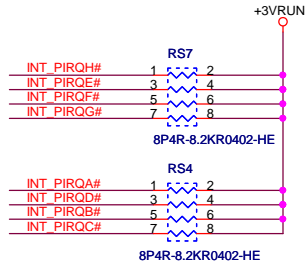
PANTHER POINT (LVDS,DDI)



PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-D	DDPD_[0]P	TMDSD_DATA2
	DDPD_[0]N	TMDSD_DATA2#
	DDPD_[1]P	TMDSD_DATA1
	DDPD_[1]N	TMDSD_DATA1#
	DDPD_[2]P	TMDSD_DATA0
	DDPD_[2]N	TMDSD_DATA0#
	DDPD_[3]P	TMDSD_CLK
	DDPD_[3]N	TMDSD_CLK#
	DDPD_AUXP	NA
	DDPD_AUXN	NA
	DDPD_HPD	HDMID_HPD
	DDPD_CTRLCLK	HDMID_CTRLCLK
	DDPD_CTRLDATA	HDMID_CTRLDATA

[illegible]

PANTHER POINT (PCI,USB,NVRAM)

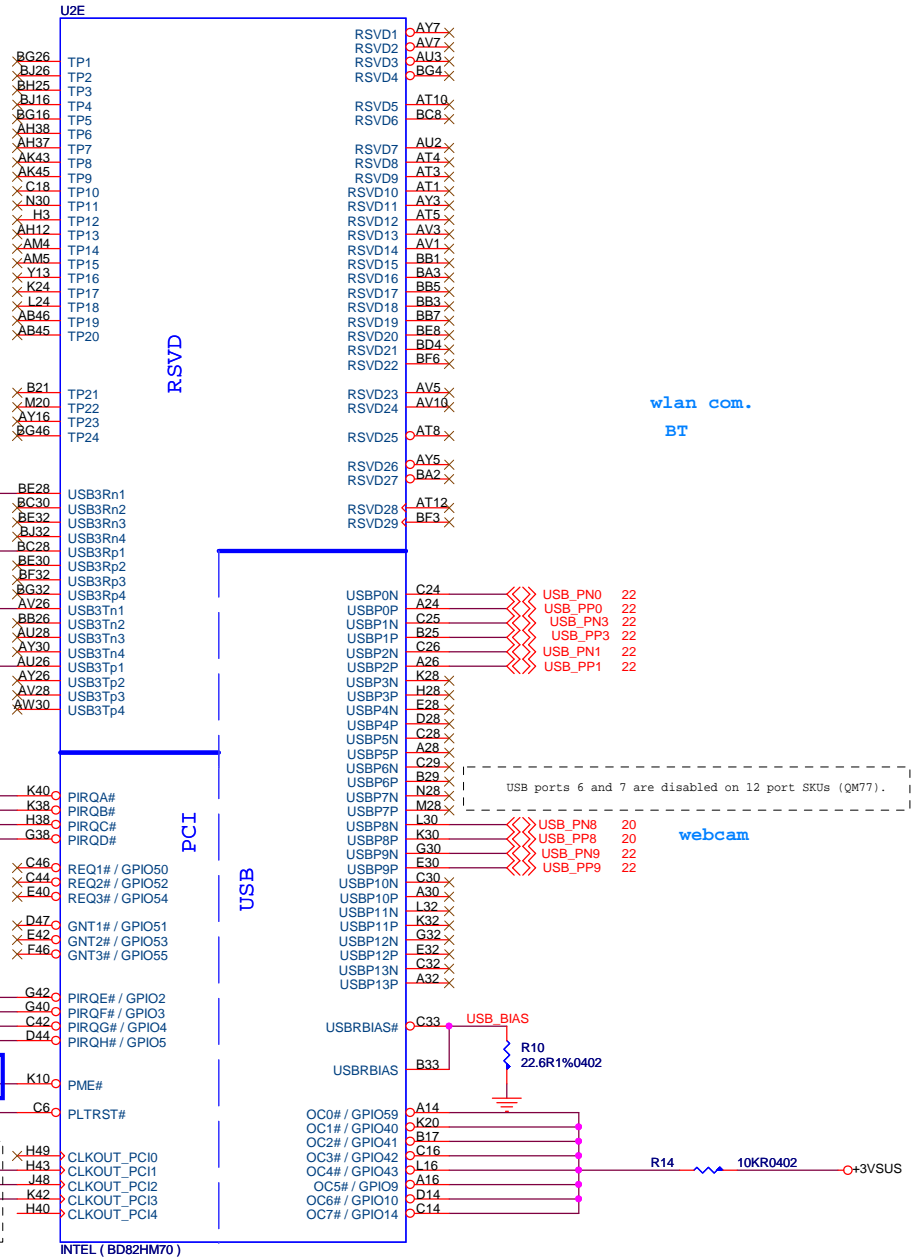
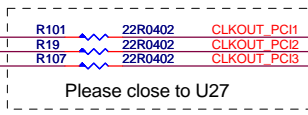
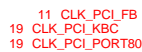
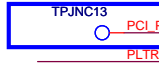
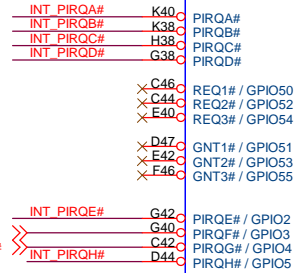
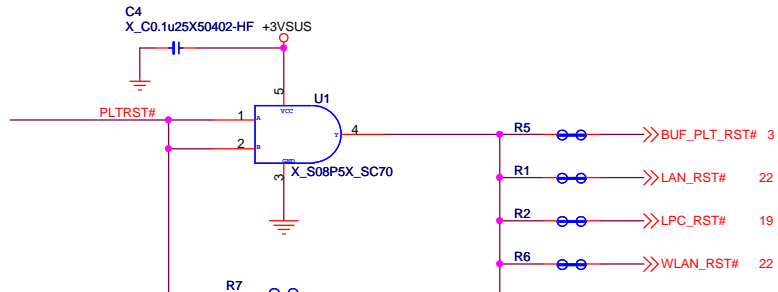
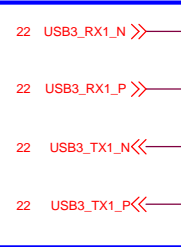


USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
BBS_BIT1 GPIO51	BBS_BIT0 GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Unsupported
1	1	SPI



GPIO35 --Define to EDID Select (If not used,require pull down)

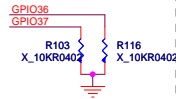
GPIO15:

This signal must be pulled up to support Intel RPAT and Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.

```

| Since Pin has strap functionality that requires -----
| internal pull-down to be sampled at rising PWROK,
| following guidelines are required to be followed:
| *When Used as SATA2GP/SATA3GP for Mechanical Presence
| detect - Use a weak external pull-up (150K-200 Kohms)
| to Vcc or PL0. Use 10K external pull-up that is enabled
| after PL0. Use PL0 as assertion - assertion
| *When Used as GP Input (Pin HW default) - Ensure GPI
| is not driven high during strap sampling window
| *When Unused as GPIO or SATA*GP - Use 8.2K-10K
| pull-down to ground.

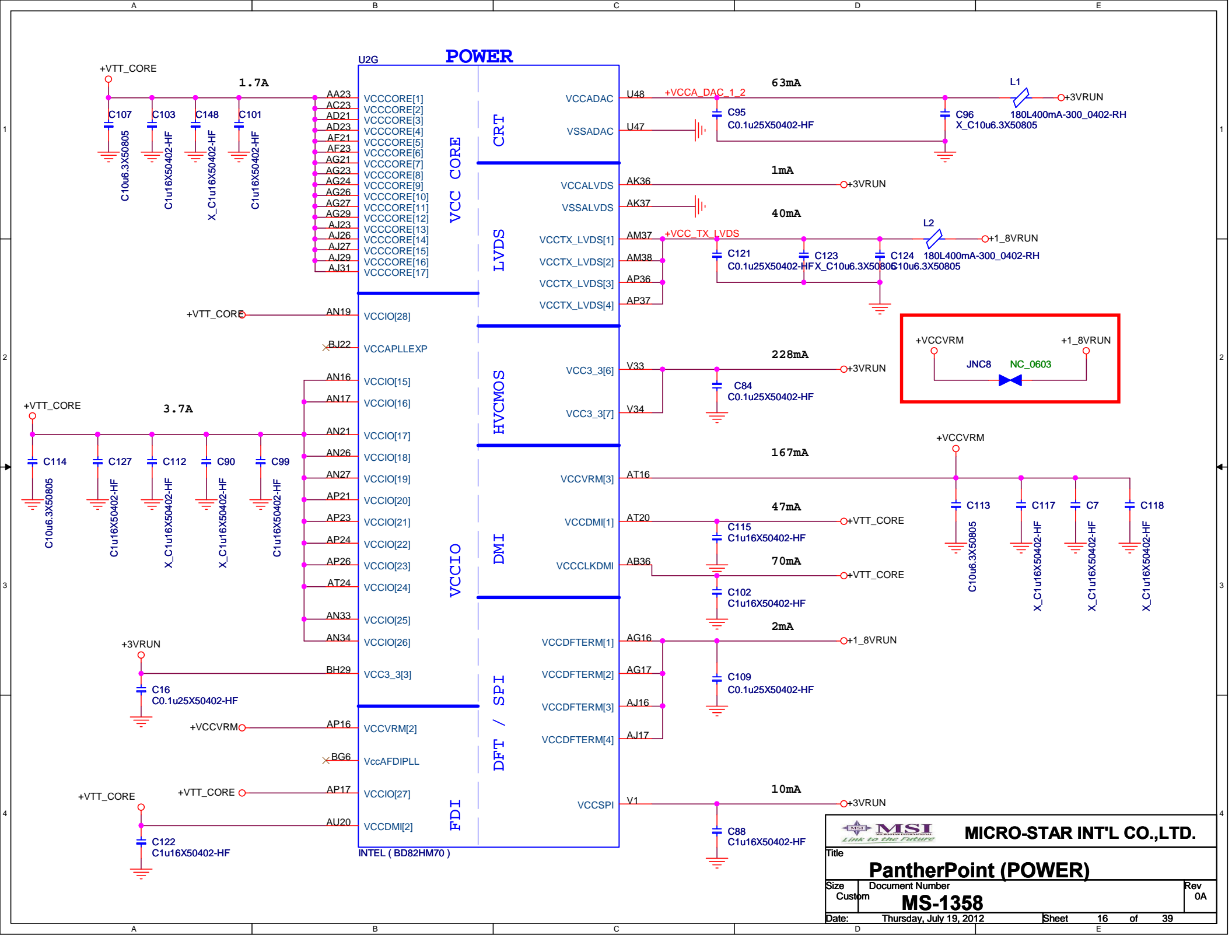
```



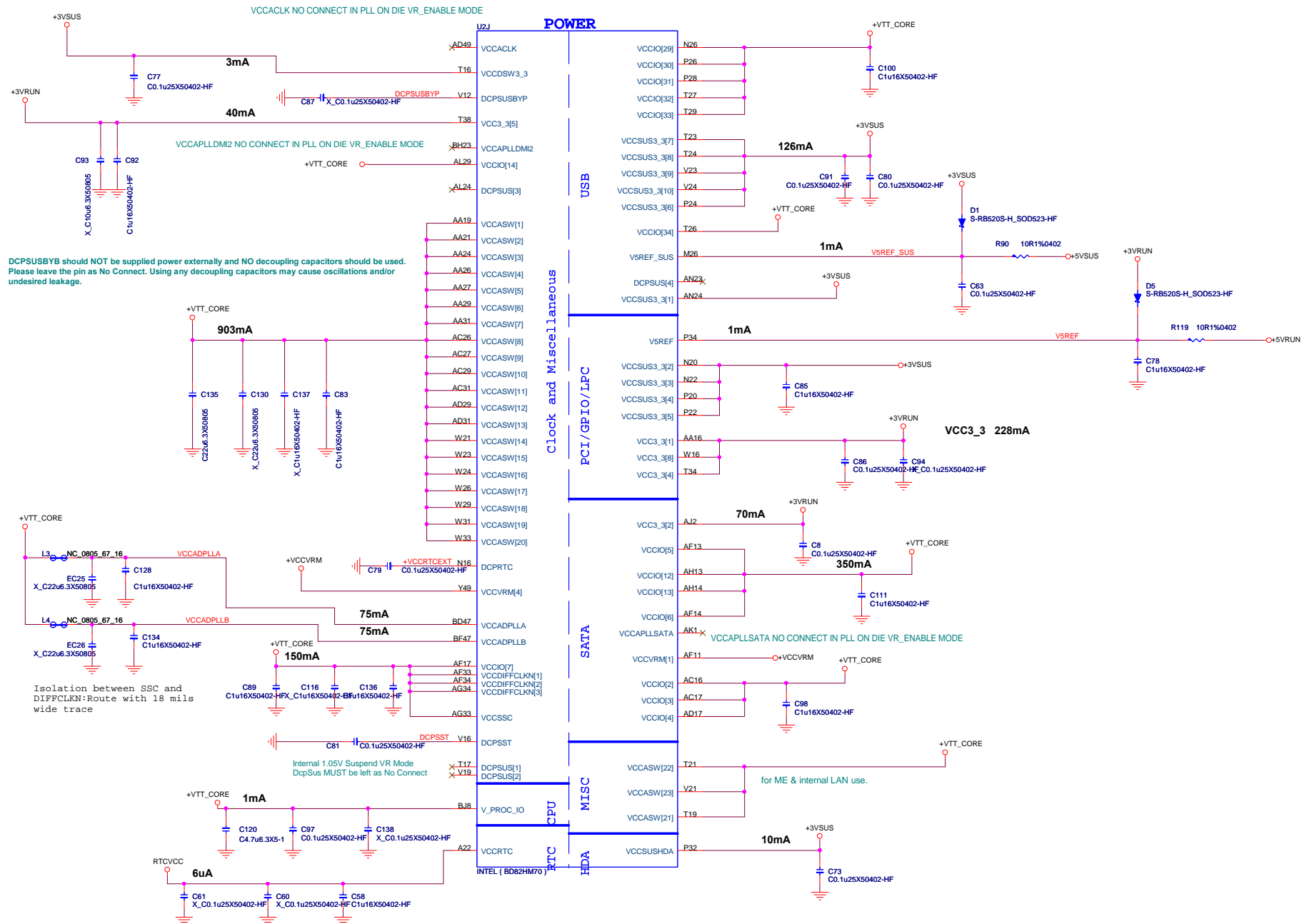
DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

Intel Comments:
Reserve 0 ohm option in these pins
pins AH8, AK11, AH10 & AK10) to GND.

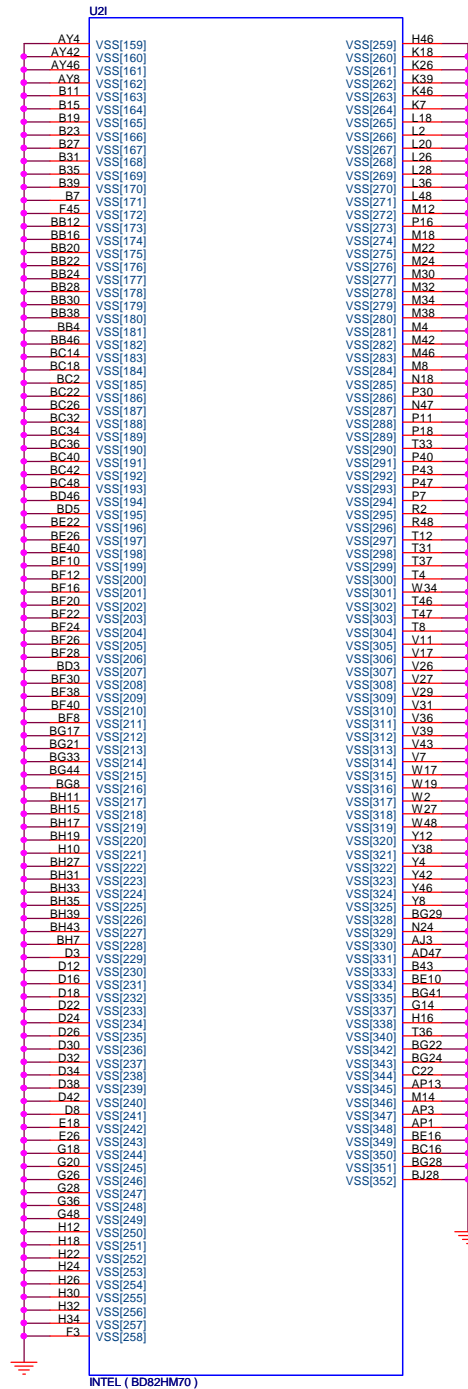
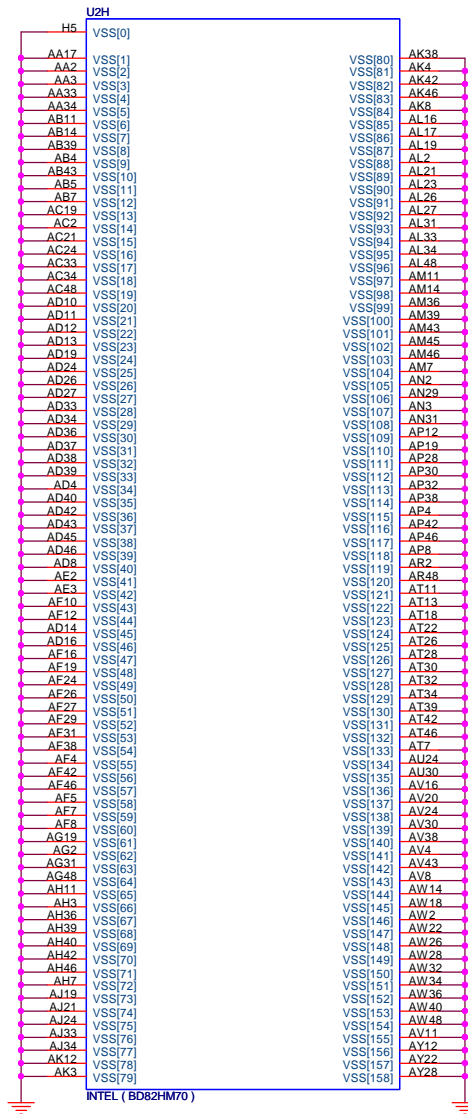
For Ivy Bridge processor only implementation:
Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor
through a 1K \pm 5% series resistor.
PROC_SELECT# also needs a 2.2K \pm 5% pull up resistor to PCH VccDFTERM
rail.

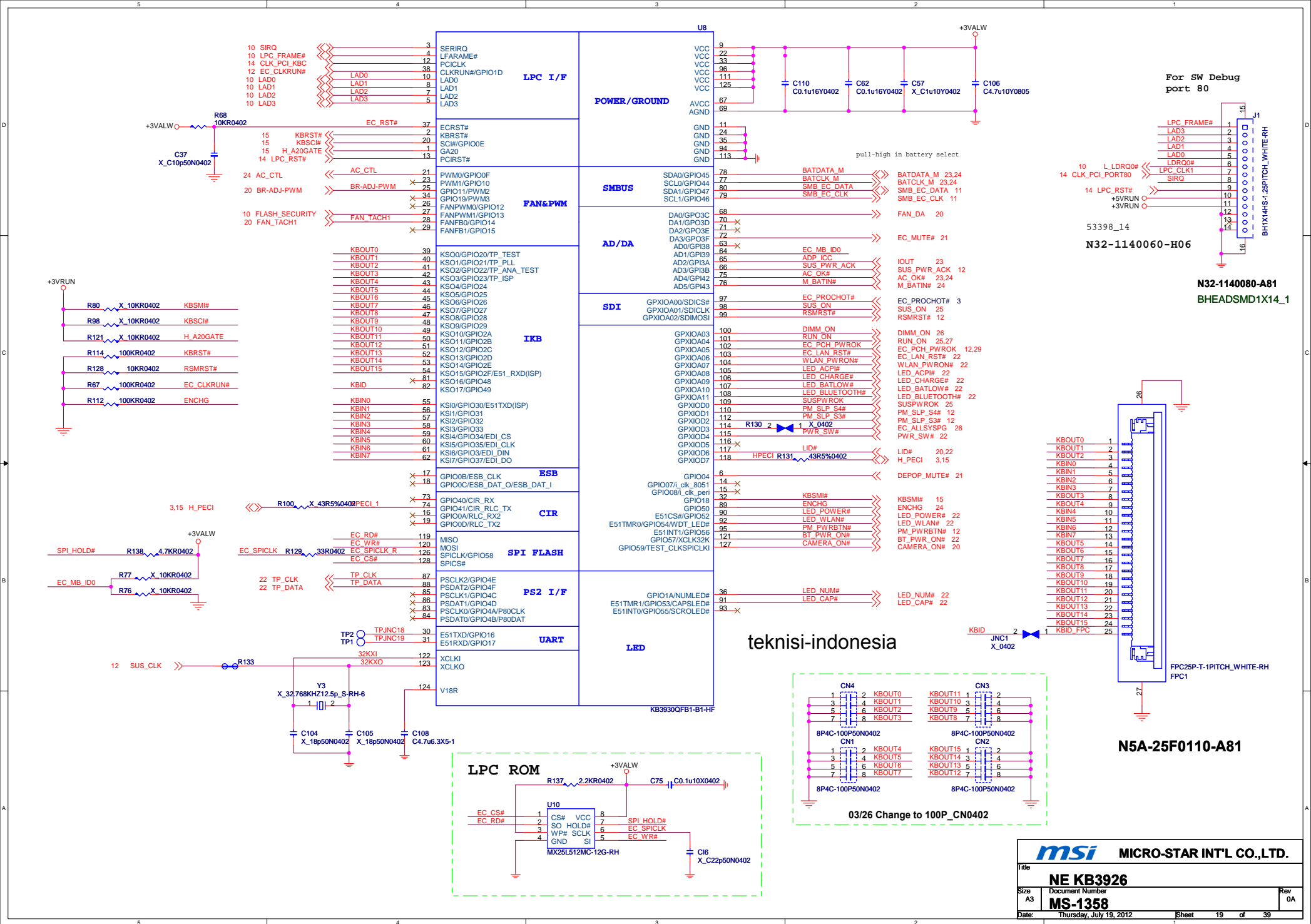


PANTHER POINT (POWER)

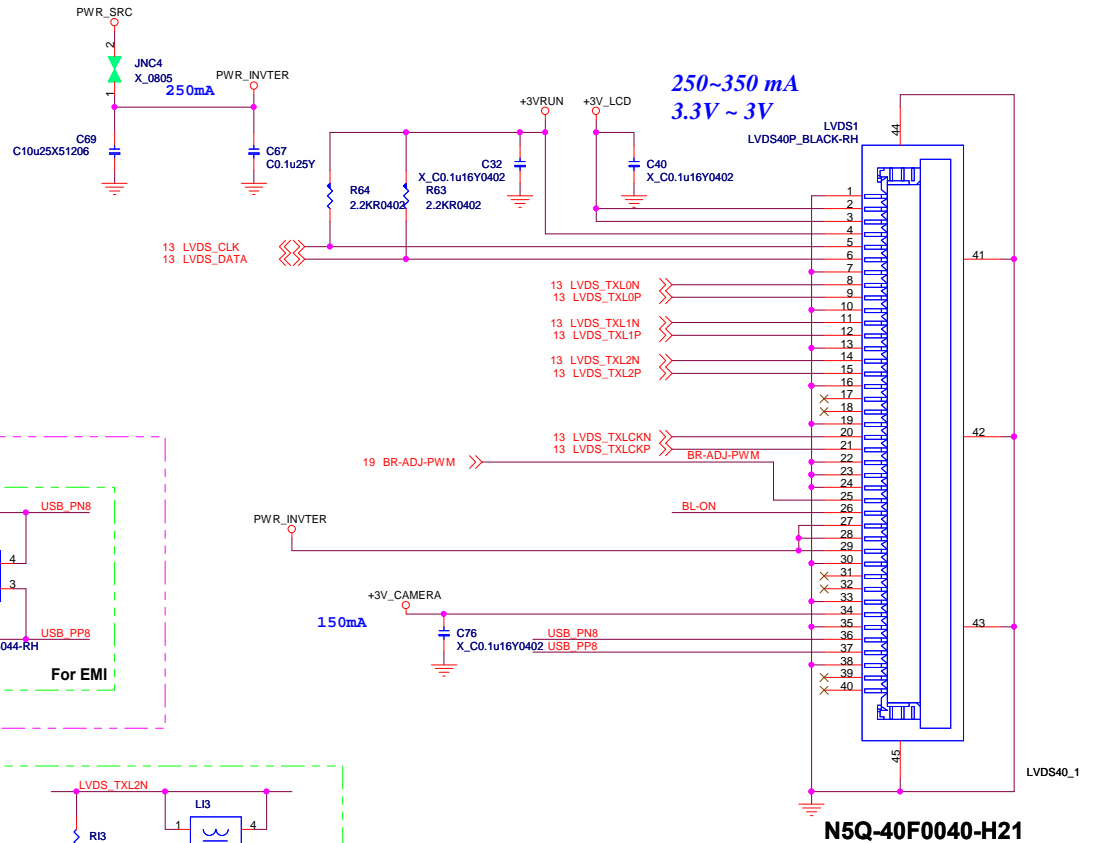
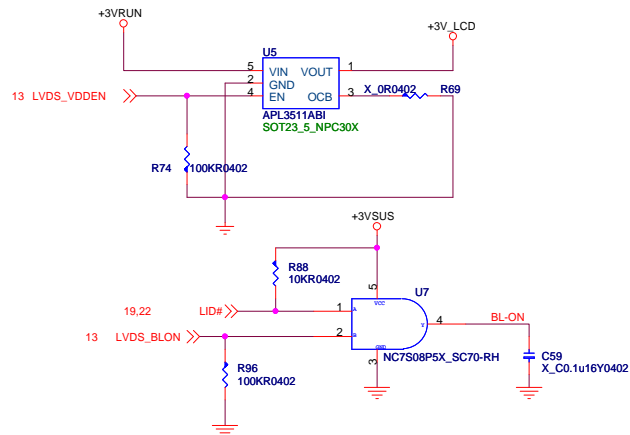


PANTHER POINT (GND)

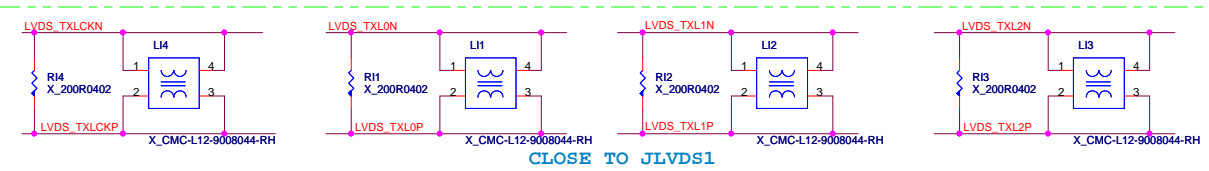
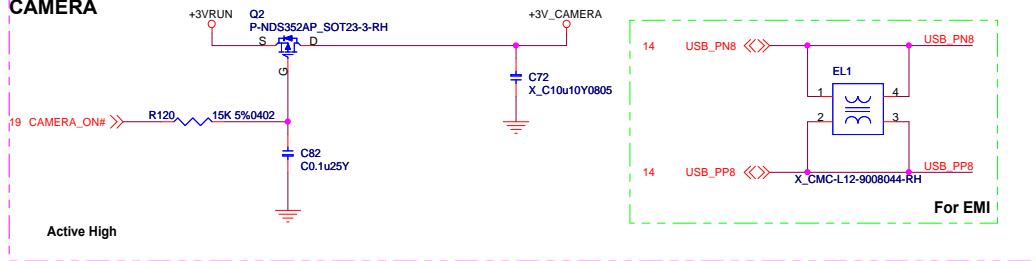




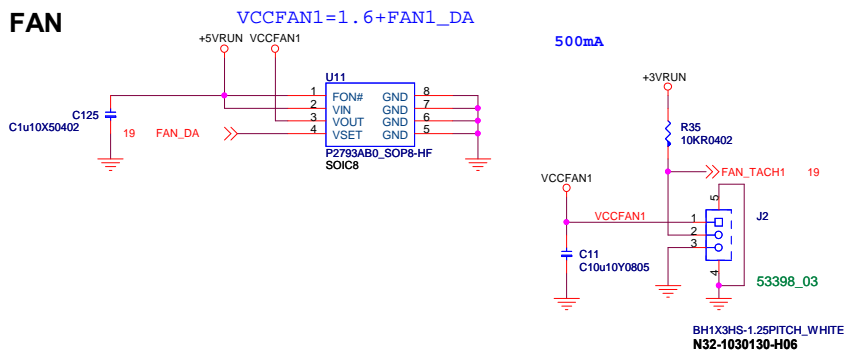
LVDS POWER



CAMERA

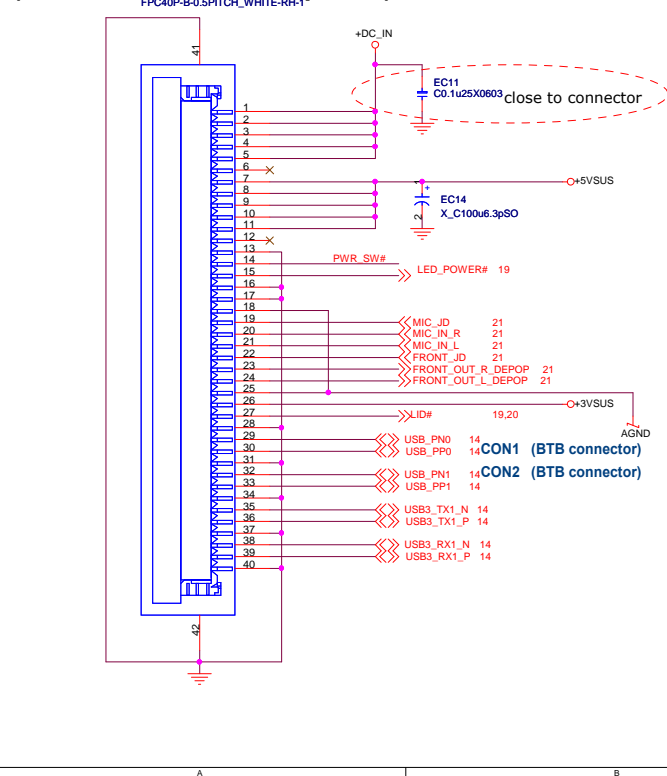


FAN

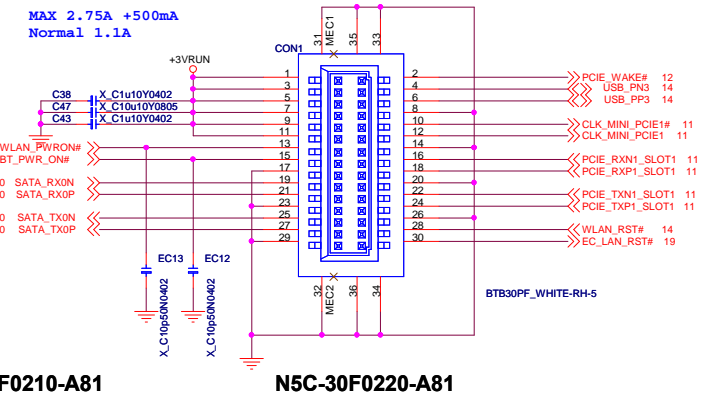
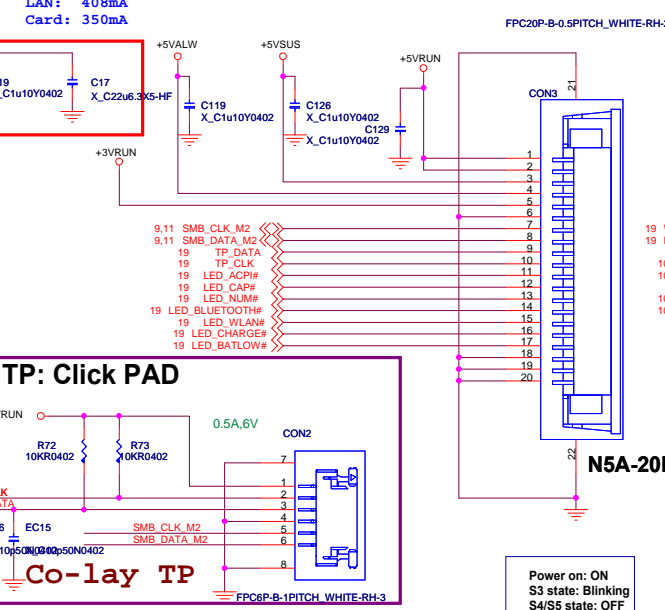


msi MICRO-STAR INT'L CO.,LTD.	
Title	
LVDS, Camera, BT, FAN	
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40PIN COAXIAL I/O Connector (USB Port x 2, MIC, Earphone)



MINI PCIE Connector

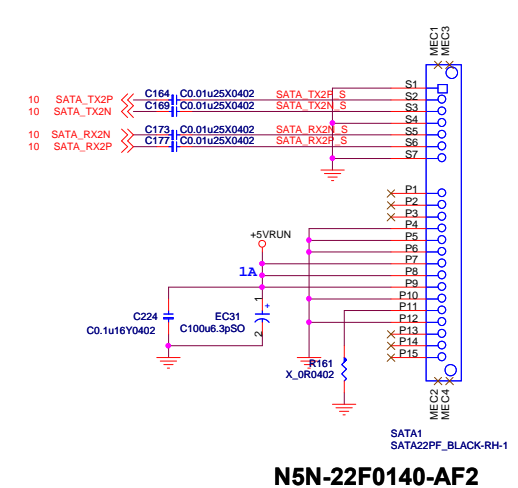


Co-lay LED

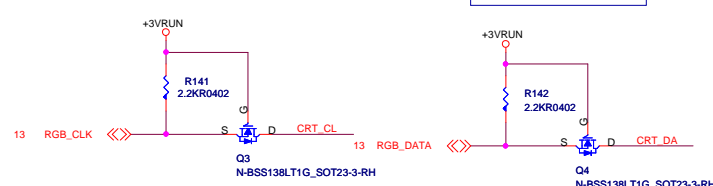
Schematic diagram for Co-lay LED connections:

- Suspend Status LED:** +5VSUS (red) → RD3 → 470R → LEDD3 → BLUE,470nm-20mA3V_1608-RH → RED ACPI#
- Cap Lock LED:** LEDD4 → BLUE,470nm-20mA3V_1608-RH → RED CAP#
- Num Lock LED:** LEDD5 → BLUE,470nm-20mA3V_1608-RH → RED NUM#
- BT LED:** LEDD7 → BLUE,470nm-20mA3V_1608-RH → RED BLUETOOTH#
- WLAN LED:** LEDD2 → LED04-WH-20mA3.15V_1608-RH → RED WLAN#
- CHARGE LED:** +5VALW (red) → RD1 → 470R → LEDD1 → BLUE,470nm-20mA3V_1608-RH → RED CHARGE#
- BATLOW LED:** RD2 → 820R → LEDD6 → BLUE,470nm-20mA3V_1608-RH → RED BATLOW#

Note: If there's no Bluetooth module, the LED of BT will be always off.



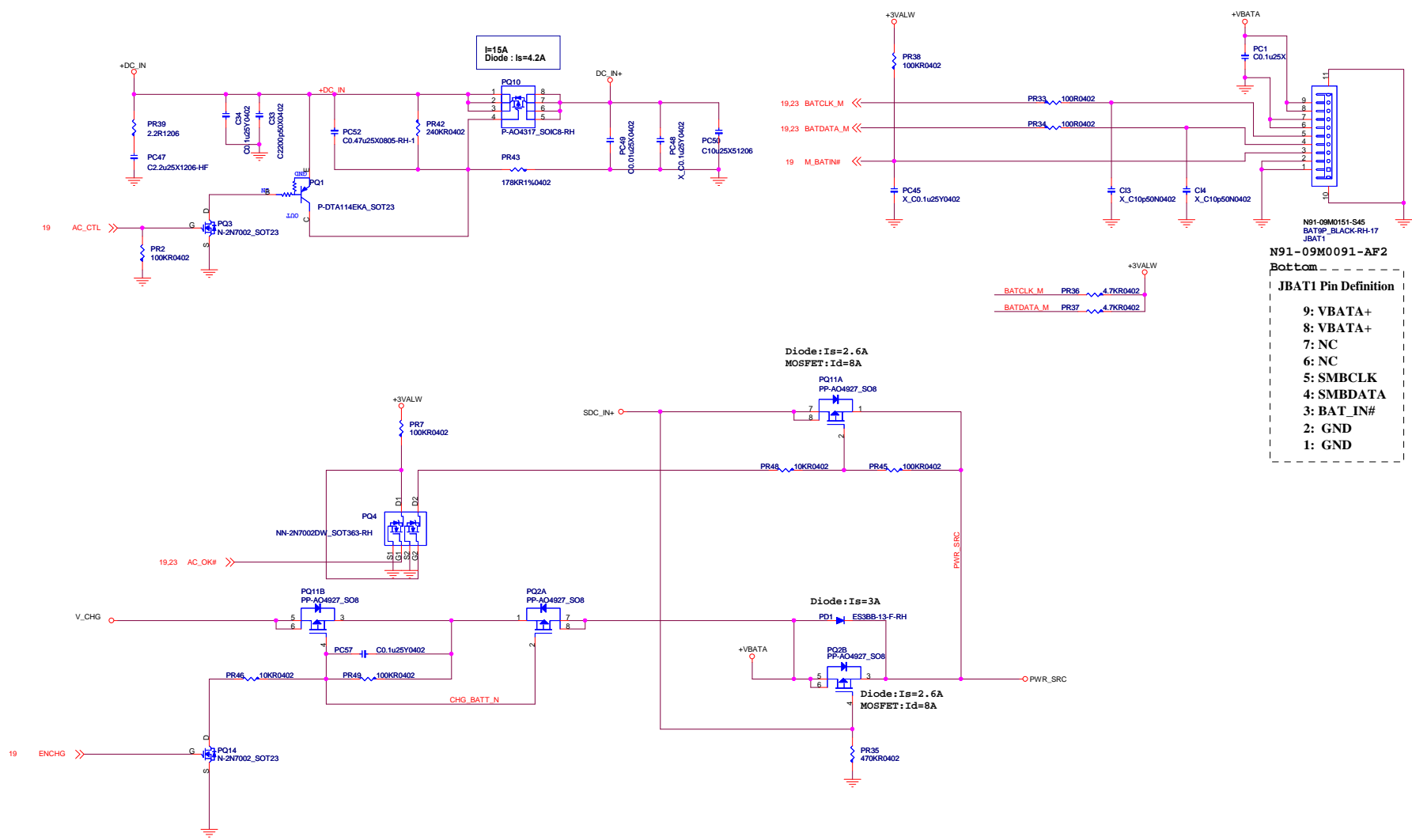
Battery Low (5%): yellow
Error: yellow Blinking
Charging: blue
Battery Full/ Discharge: OFF



 MICRO-STAR INT'L CO.,LTD.	
Title	
HDD, BTB CON	
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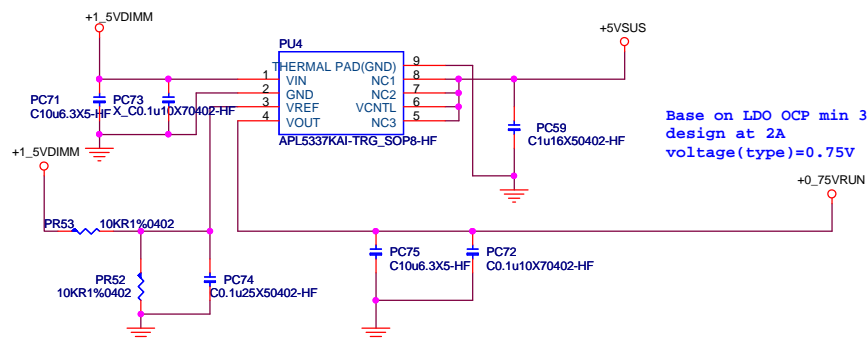
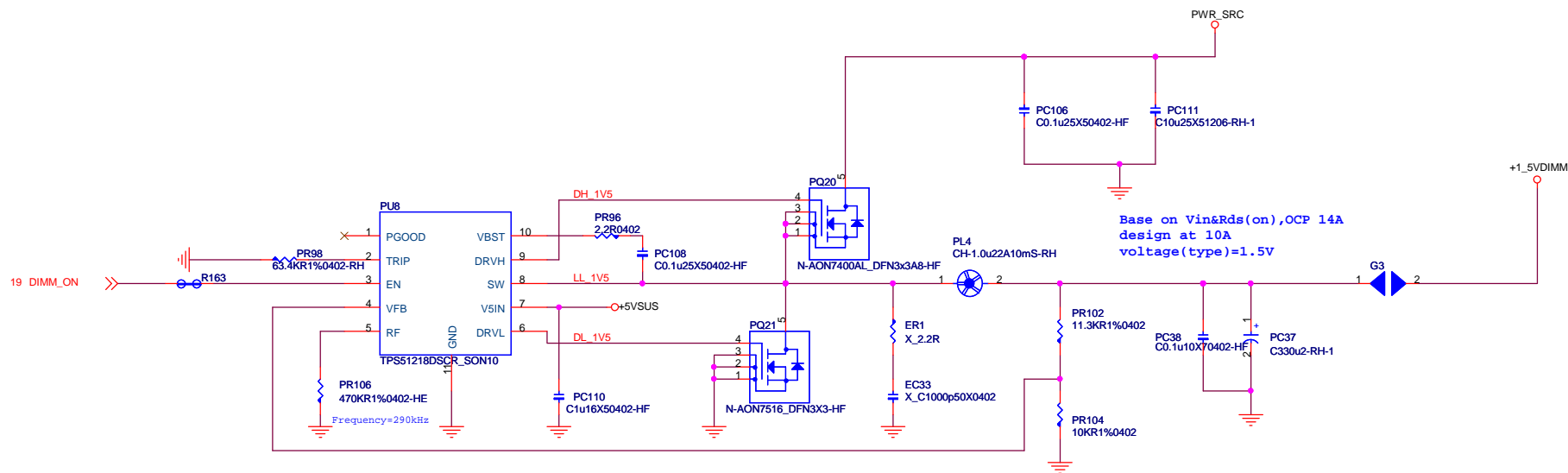
Adapter input voltage set 19 Voltage




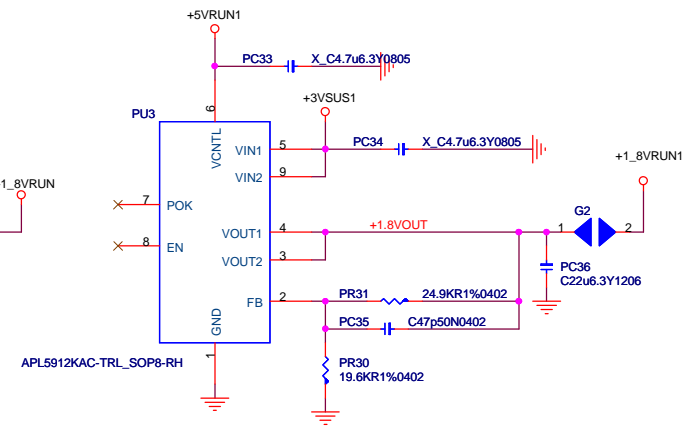
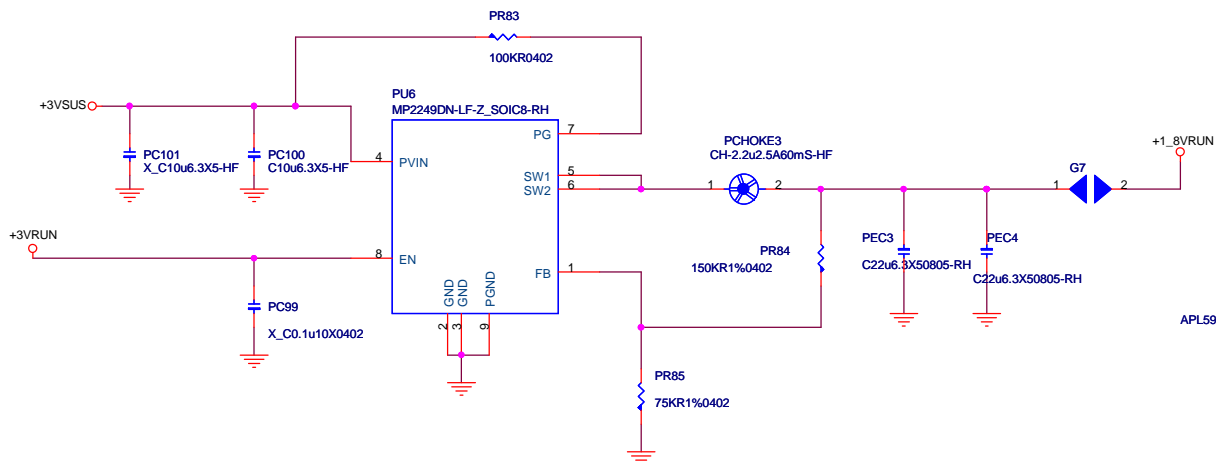
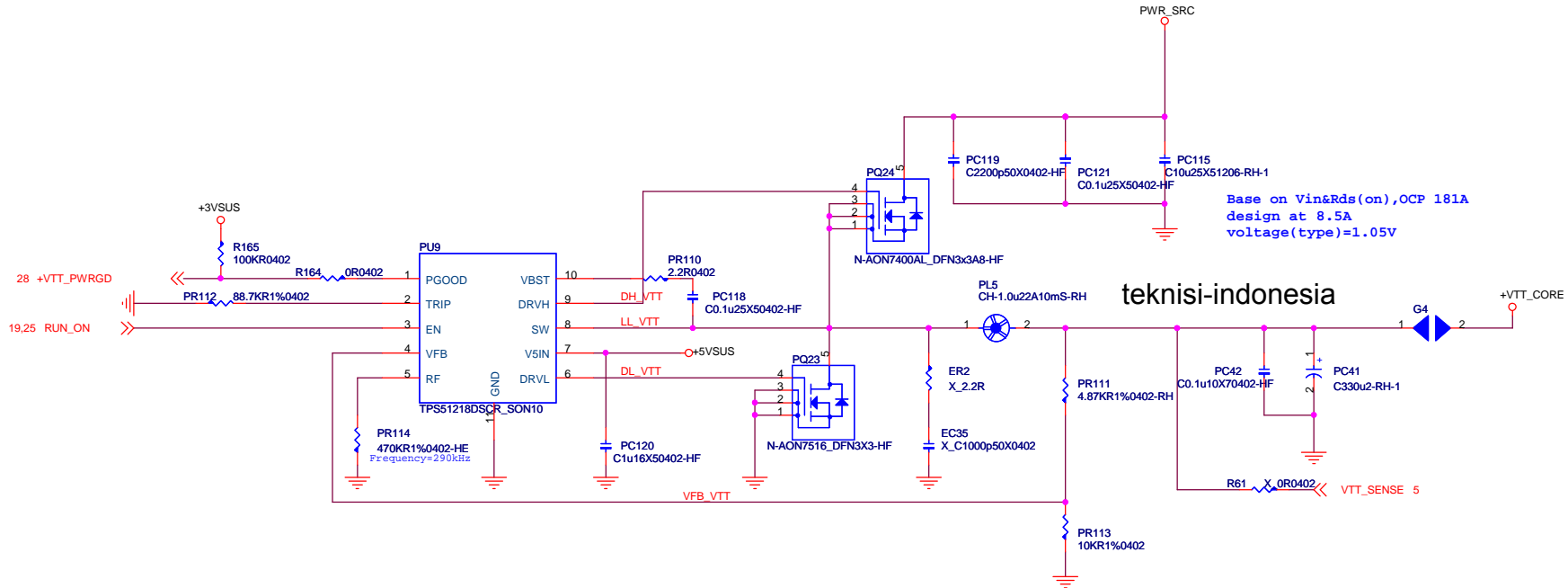



N91-09M0091-AF2
Bottom
JBAT1 Pin Definition

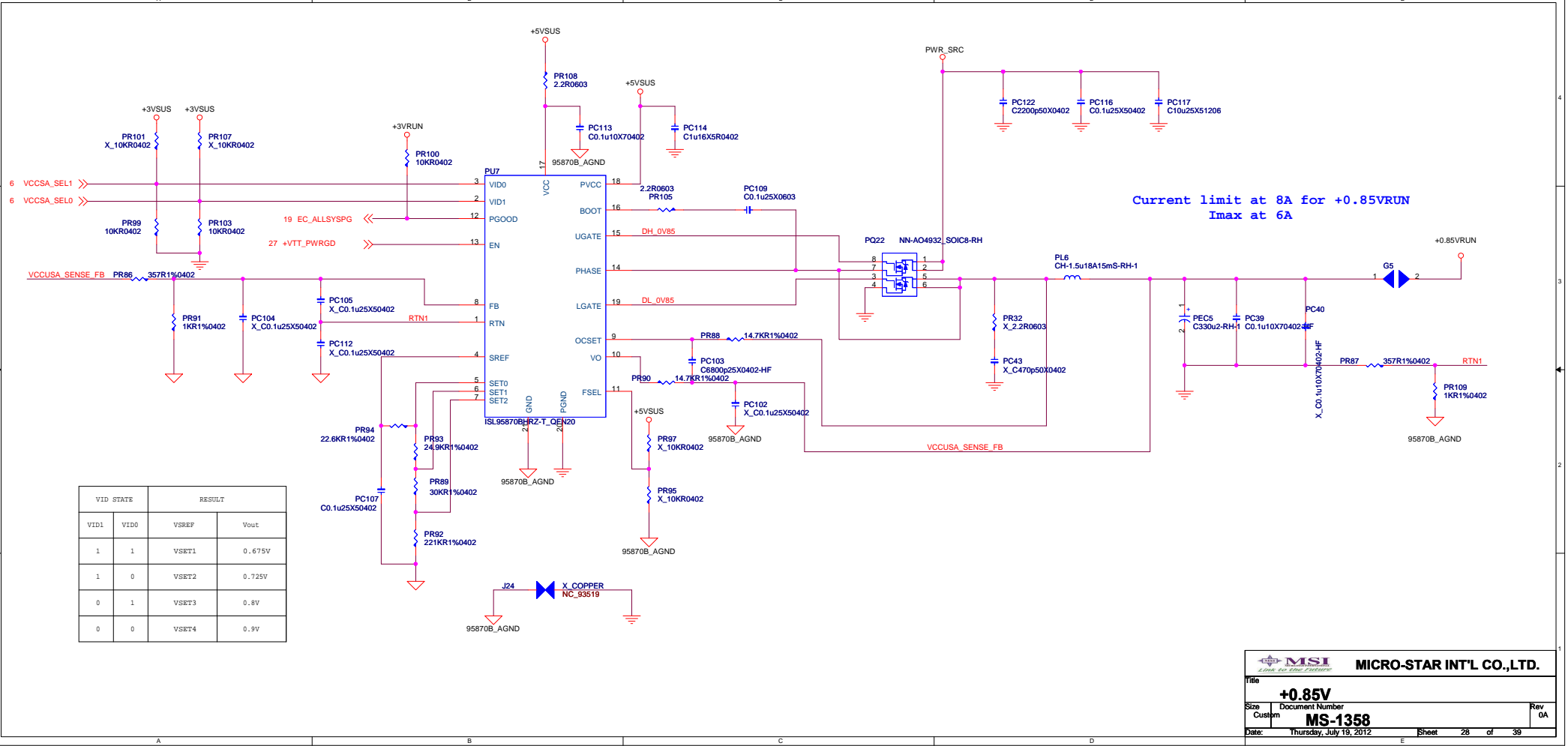
- 9: VBATA+
- 8: VBATA+
- 7: NC
- 6: NC
- 5: SMBCLK
- 4: SMBDATA
- 3: BAT_IN#
- 2: GND
- 1: GND



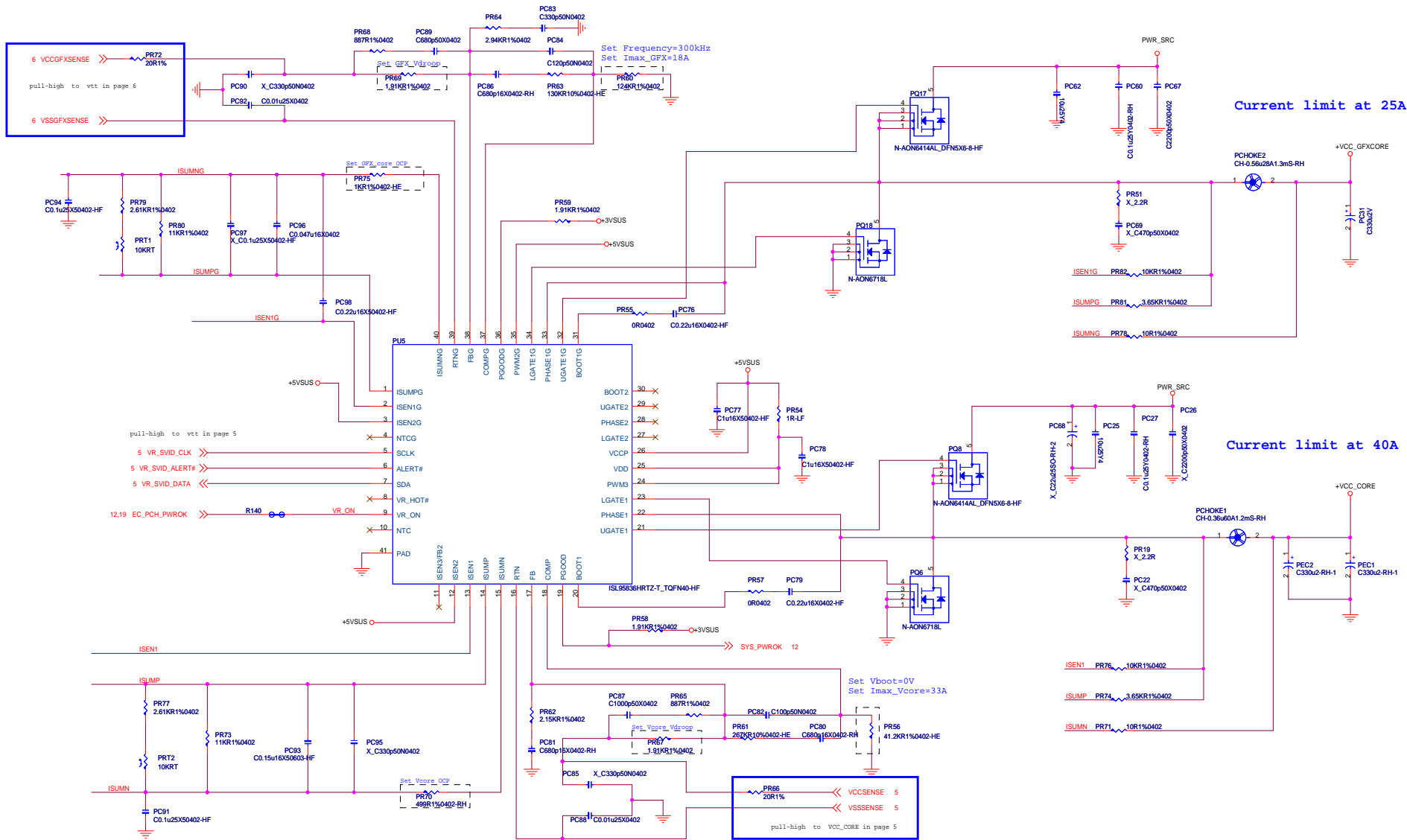
 MICRO-STAR INT'L CO.,LTD.	
Title	
DIMM & SMDR VTERM	
Size	Document Number
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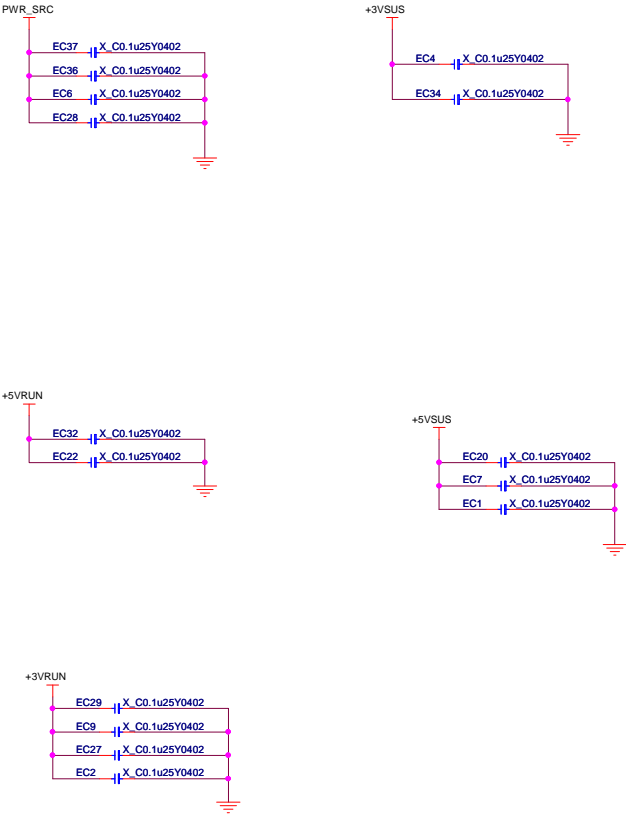
 MICRO-STAR INT'L CO.,LTD.	
Title	
+VTT & +1.05VLAN	
Size	Document Number
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VID STATE		RESULT	
VID1	VID0	VSREF	Vout
1	1	VSET1	0.675V
1	0	VSET2	0.725V
0	1	VSET3	0.8V
0	0	VSET4	0.9V

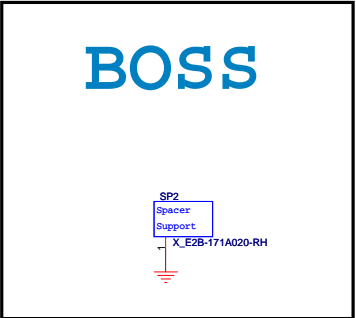
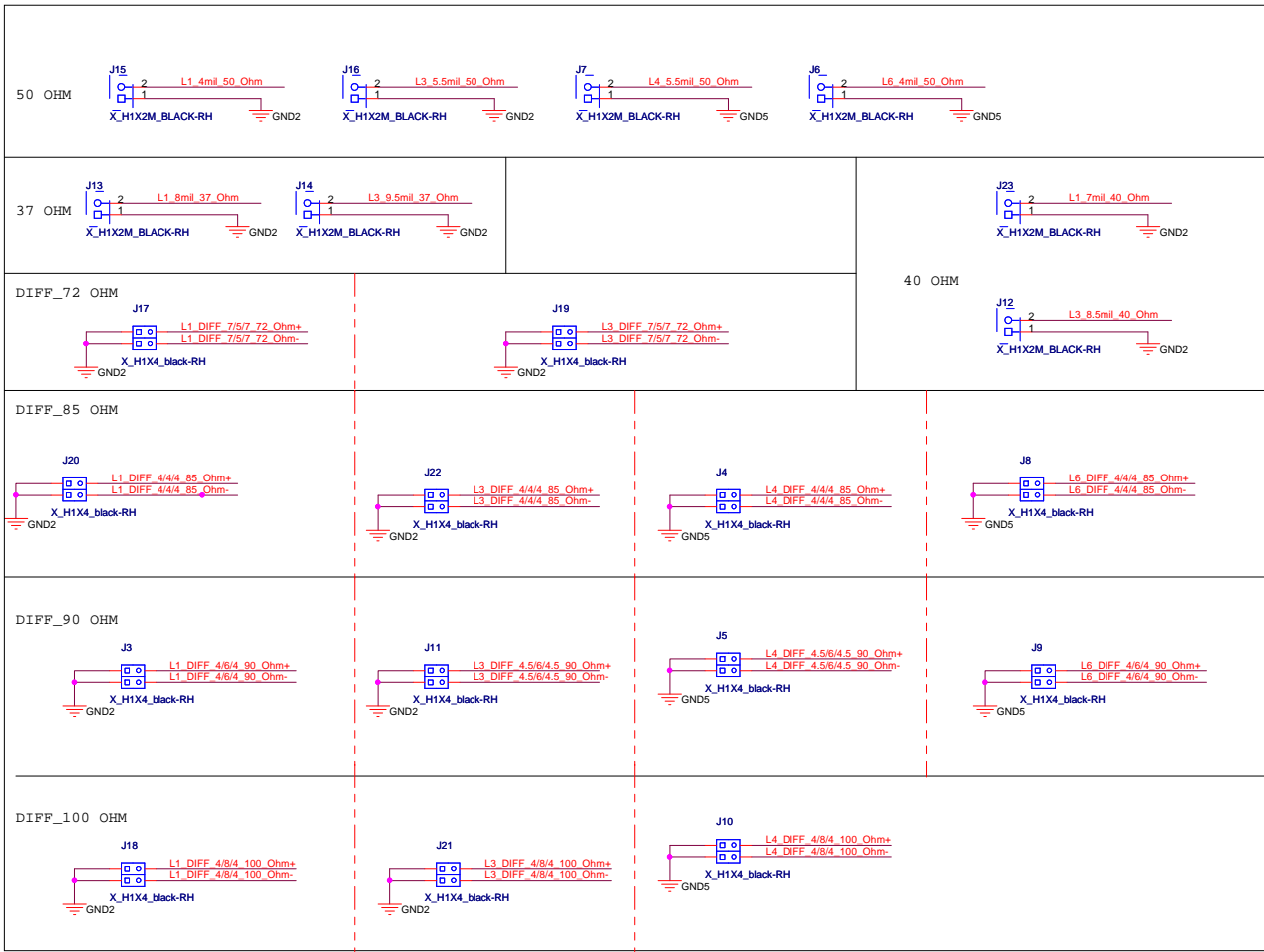
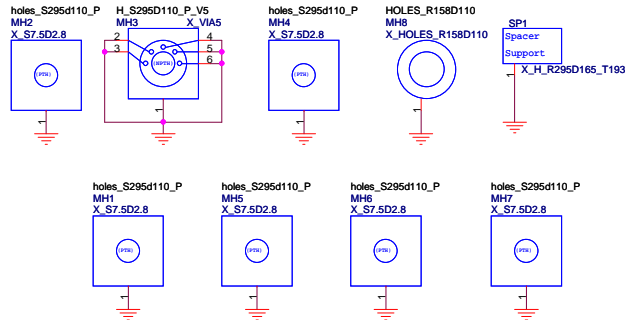
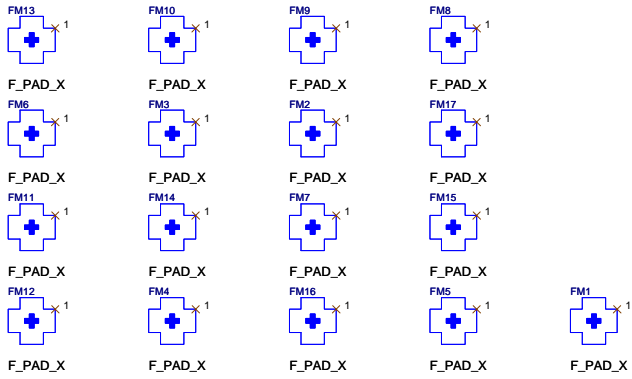
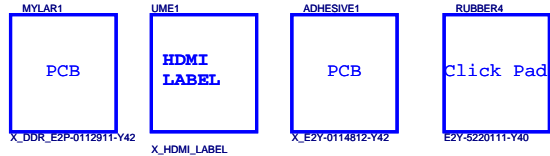
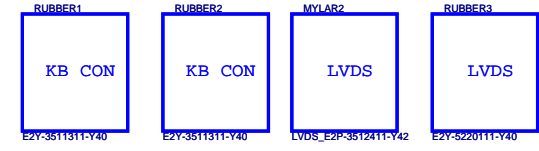


EMI SOLUTION

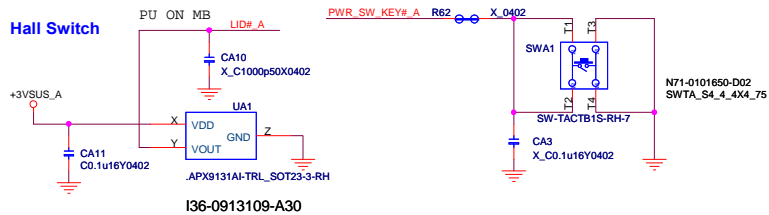




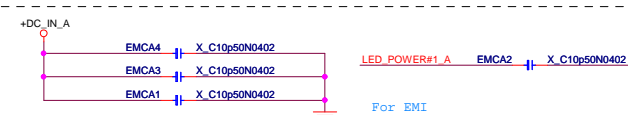
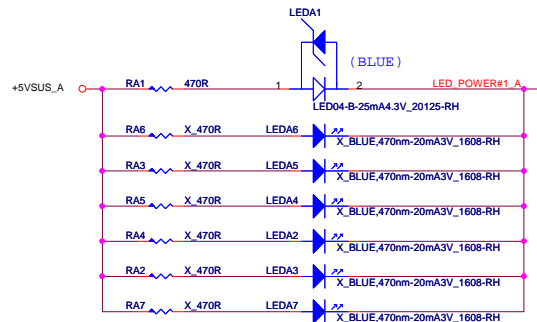
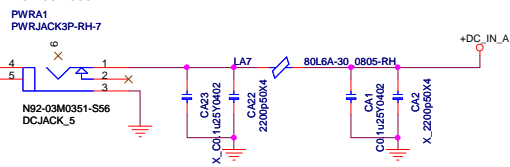
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P30-135810A-T53,



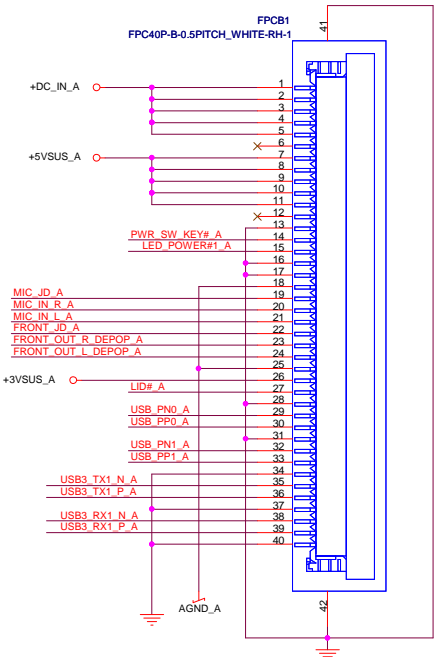
Hall Switch



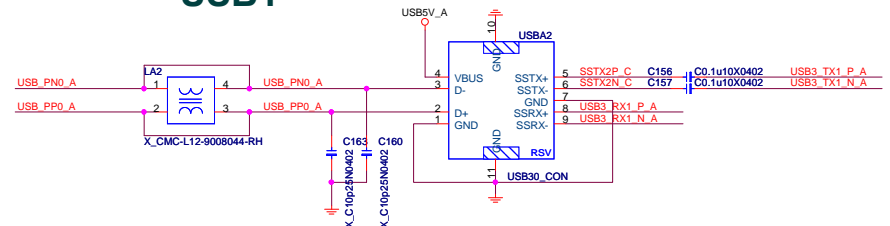
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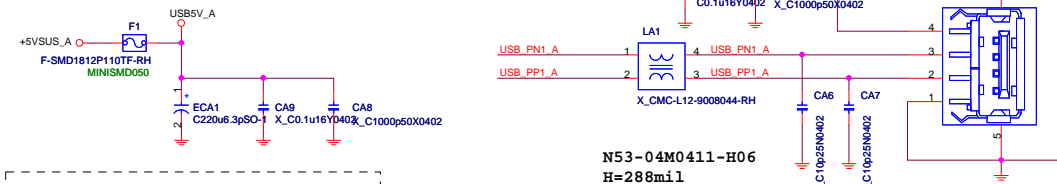
40PIN COAXIAL I/O Connector



USB1



USB2



msi

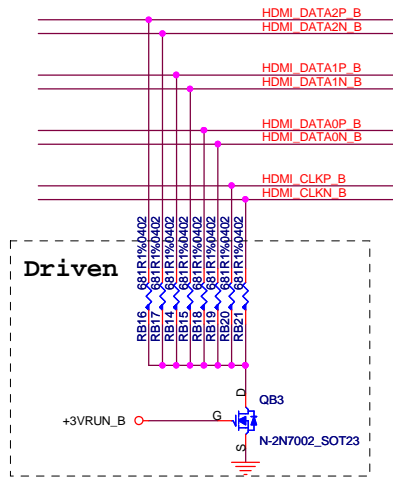
MICRO-STAR INT'L CO.,LTD.

Title DCIN/AUDIO JACK/USB/CONN

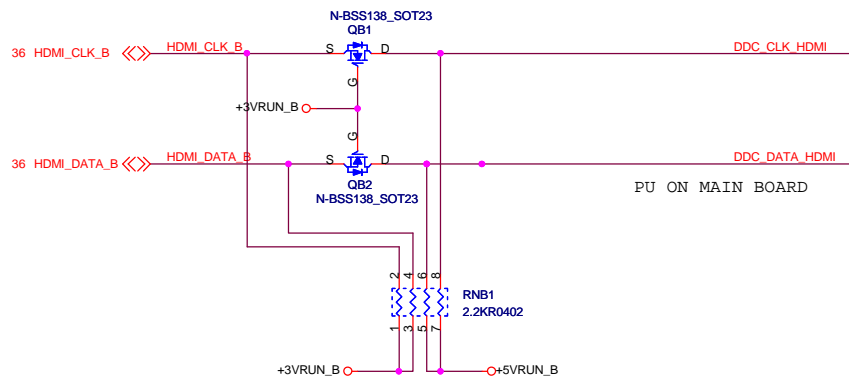
Size Document Number MS-1358

Date Thursday, July 19, 2012

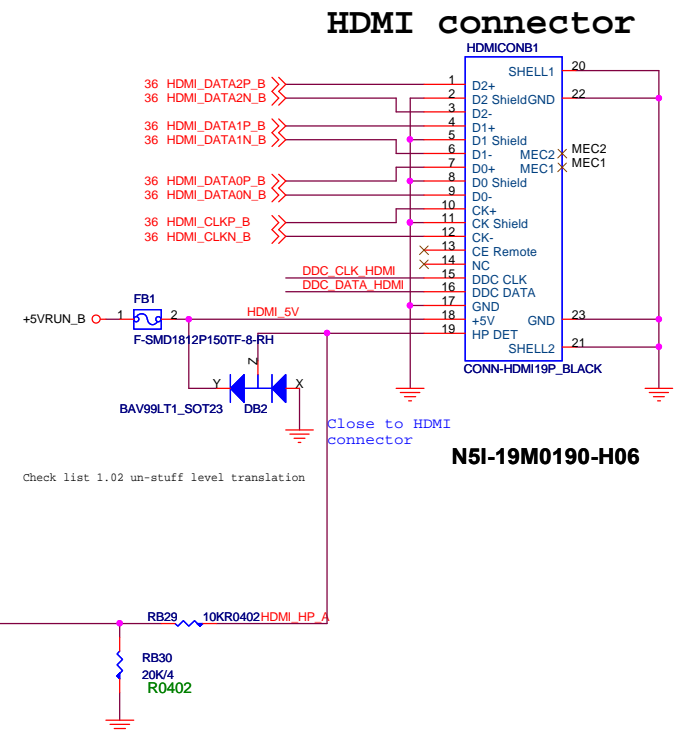
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CHECK LIST 499 ohm or amd errata 750 ohm



PU ON MAIN BOARD

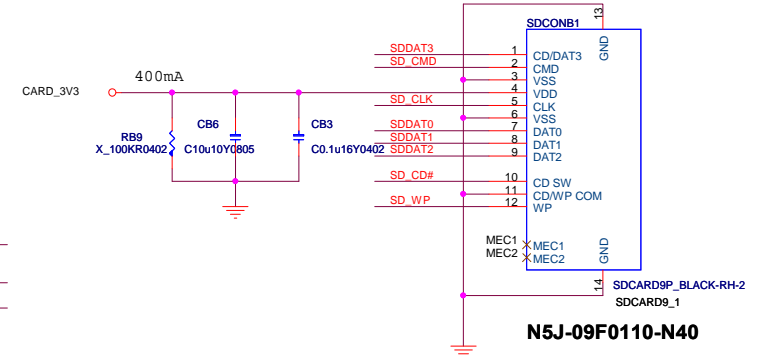
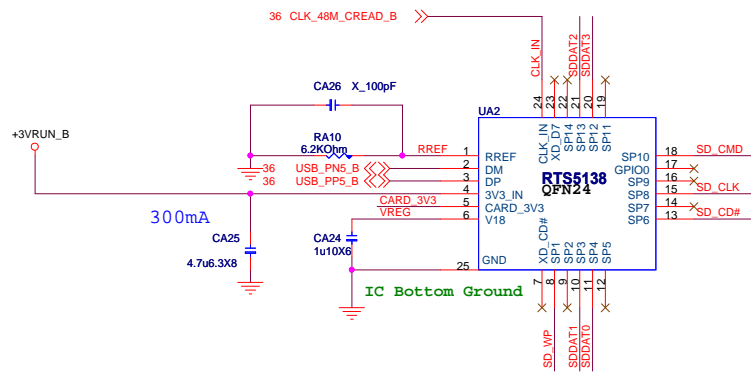


HDMI connector

N5I-19M0190-H06

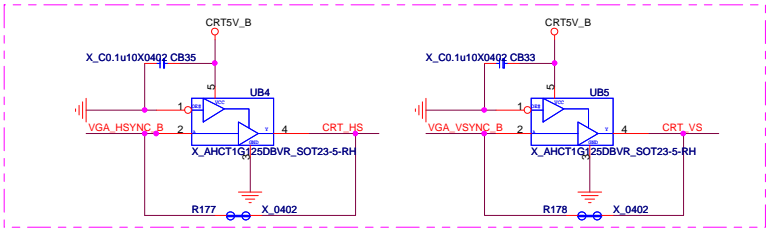
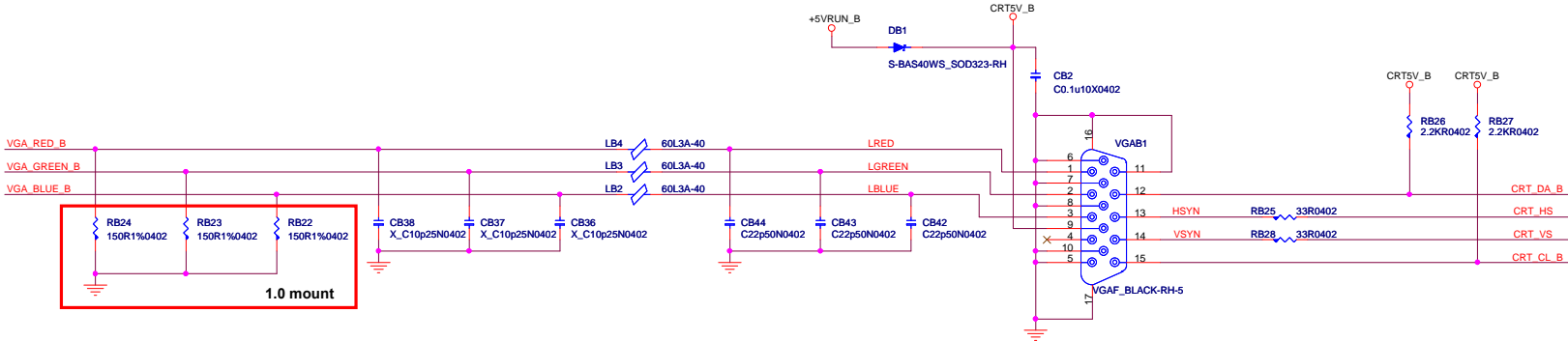
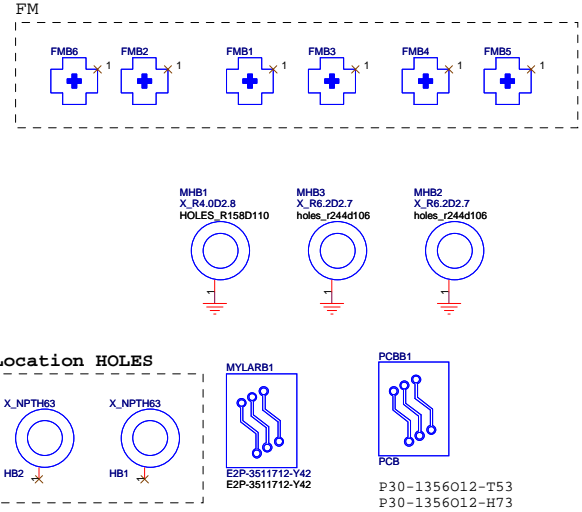
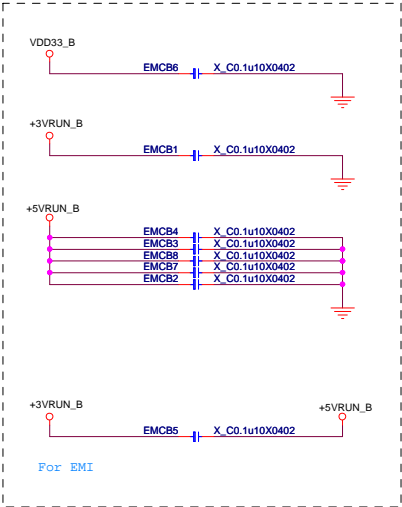
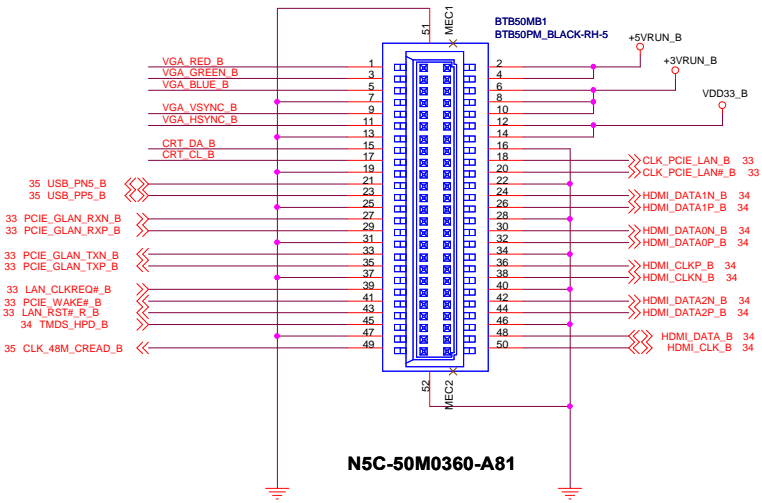
msi MICRO-STAR INT'L CO.,LTD.	
Title	
HDMI Connector	
Size B	Document Number
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1	

Card Reader controller RTS 5138



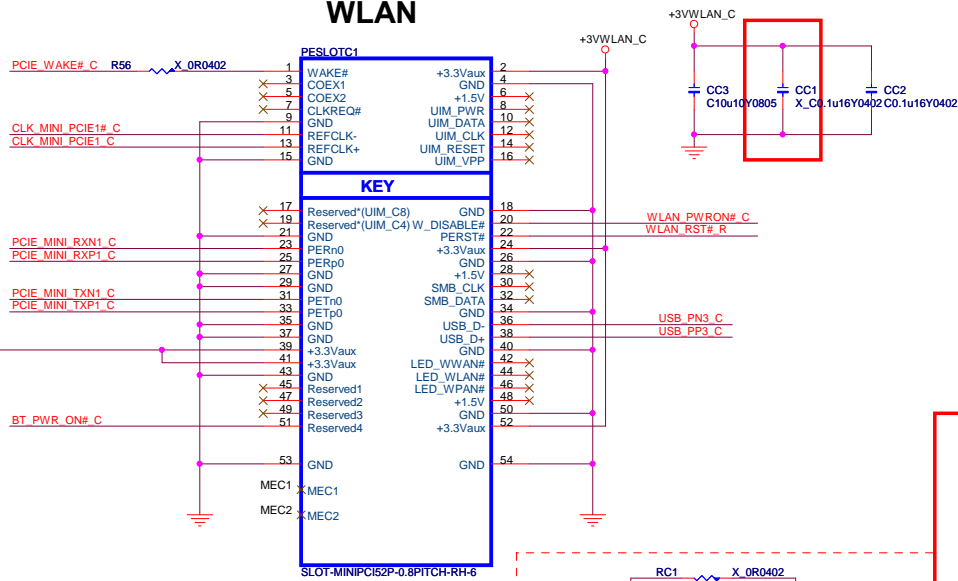
Clock	MODE1	MODE0
48MHz	X	X
24MHz	X	○
12MHz (Crystal)	○	○

50PIN BTB I/O Connector ㄟ



msi MICRO-STAR INT'L CO.,LTD.	
Title	CRT/CONNECTOR
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WLAN

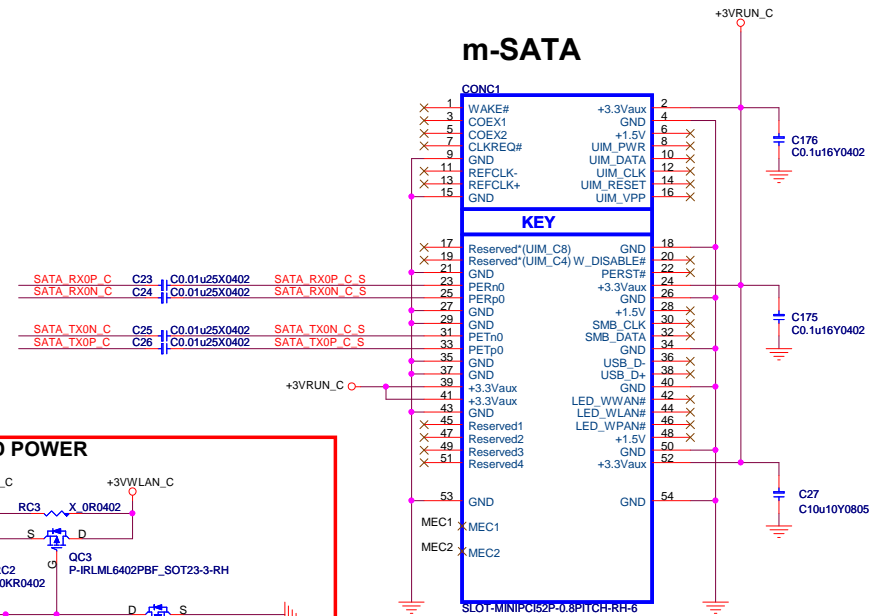


N11-0520450-L41

AW-NE785H Pin-out Definitions

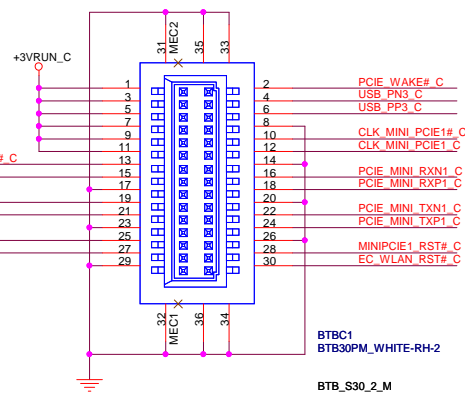
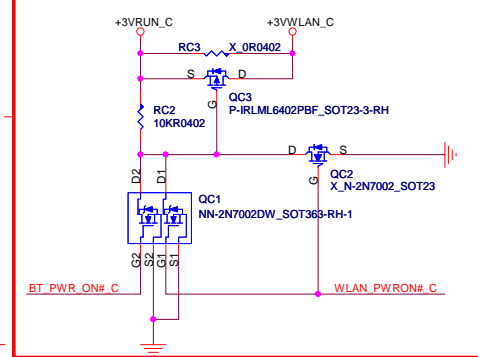
Pin No.	Definition	Basic Description	Type
1	NC	No connect. Should be left open.	
2	3.3v	3.3V power supply	VCC
3	NC	No connect. Should be left open	
4	GND	Ground	GND
5	NC	No connect. Should be left open	
6	NC	No connect. Should be left open.	
7	CLKREQ_L	Reference clock request.	
8	NC	No connect. Should be left open.	
9	GND	Ground	GND
10	NC	No connect. Should be left open.	
11	REFCLK-	Differential reference clock	
12	NC	No connect. Should be left open.	
13	REFCLK+	Differential reference clock	
14	NC	No connect. Should be left open.	
15	GND	Ground	GND
16	NC	No connect. Should be left open.	
17	NC	No connect. Should be left open.	
18	GND	Ground	GND
19	NC	No connect. Should be left open.	
20	W_DISABLE_L	WLAN disable control.	Input
21	GND	Ground	GND
22	PERST_L	PCI express fundamental reset	Input
23	PERn0	Differential transmit	Output
24	NC	No connect. Should be left open.	
25	PERp0	Differential transmit	Output
26	GND	Ground	GND
27	GND	Ground	GND
28	NC	No connect. Should be left open.	
29	GND	Ground	GND
30	NC	No connect. Should be left open.	
31	PETn0	Differential receive	Input
32	NC	No connect. Should be left open.	
33	PETp0	Differential receive	Input
34	GND	Ground	GND
35	GND	Ground	GND
36	NC	No connect. Should be left open.	
37	GND	Ground	GND
38	NC	No connect. Should be left open.	
39	NC	No connect. Should be left open.	
40	GND	Ground	GND
41	NC	No connect. Should be left open.	
42	NC	No connect. Should be left open.	
43	NC	No connect. Should be left open.	
44	LED_WLAN_L	Active low signal. The signal is used to provide status indicators via LED.	Output
45	NC	No connect. Should be left open.	
46	NC	No connect. Should be left open.	
47	NC	No connect. Should be left open.	
48	NC	No connect. Should be left open.	
49	NC	No connect. Should be left open.	
50	GND	Ground	GND
51	NC	No connect. Should be left open.	
52	3.3v	3.3V power supply	VCC

m-SATA

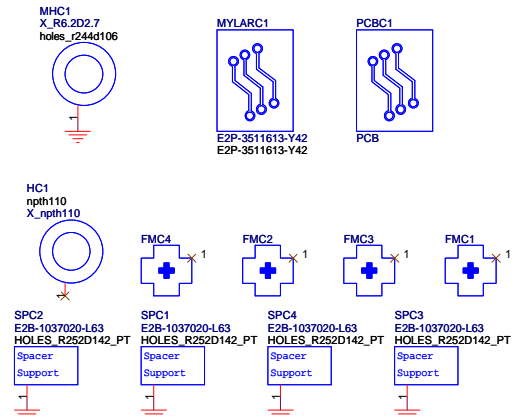


N11-0520210-K06

MINICARD POWER

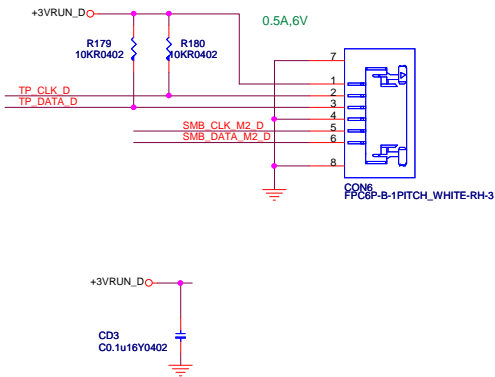


N5C-30M0130-A81

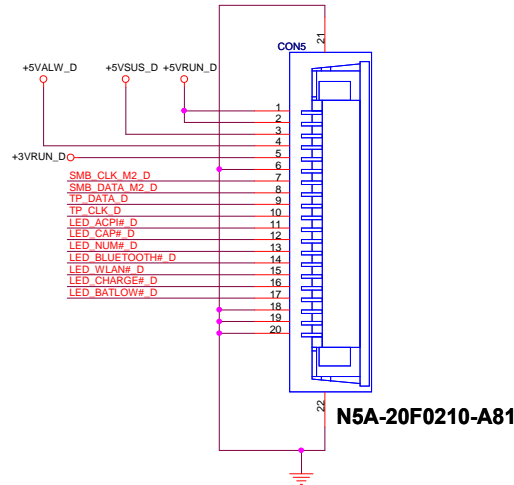


Title		
MINIPCI Board		
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TP: Click PAD



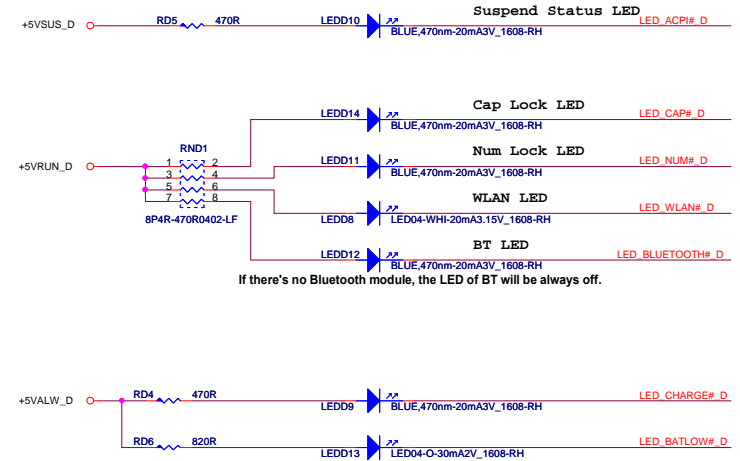
Launch Board CONN



teknisi-indonesia

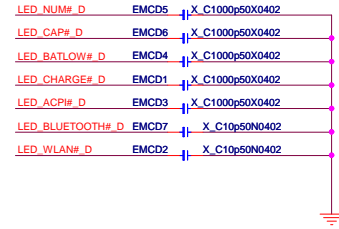
LED Location

Top View left to right side

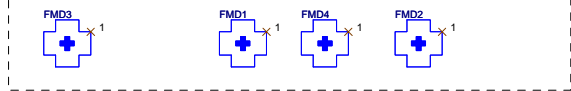


Power on: ON
S3 state: Blinking
S4/S5 state: OFF

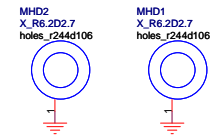
Battery Low (5%): yellow
Error: yellow Blinking
Charging: blue
Battery Full/ Discharge: OFF



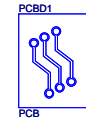
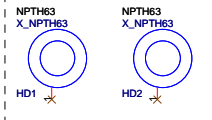
FM



SCREW HOLES



Location HOLES



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Title		
Launch+TP Board		
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